Current-Mode High-Accuracy High-Precision CMOS Amplifiers

Christian Falconi, *Member, IEEE*, Giuseppe Ferri, *Senior Member, IEEE*, Vincenzo Stornelli, *Student Member, IEEE*, Andrea De Marcellis, Daniele Mazzieri, and Arnaldo D'Amico

***Abstract*—In low-voltage, deep sub- μm analog CMOS circuits, the accuracy and precision can be limited by the finite gain as well as by the input offset and $1/f$ noise voltages of opamps. Here, we show how to design high-accuracy high-precision CMOS amplifiers by properly applying dynamic element matching to a second-generation current conveyor (CCII); if all of the critical, nominally identical transistor pairs are dynamically matched, the resulting amplifier has low residual input offset and noise voltages. When compared with chopper or traditional dynamic element-matching amplifiers, the proposed approach alleviates the tradeoff between output swing and output resistance and is more robust against the finite opamp gain. Transistor-level simulations confirm theoretical results.**

***Index Terms*—Current-mode amplifiers, second-generation current conveyor (CCII), dynamic element matching (DEM), deep sub- μm CMOS microsystems.**

I. Introduction

THE trend toward low-voltage low-power CMOS analog circuits [1]–[4] has made it more and more difficult to design high-accuracy high-precision electronic interfaces [5].

In fact, although standard CMOS processes may offer several advantages (e.g., low cost, low power consumption, and compatibility with digital subsystems), CMOS opamps typically exhibit rather high input offset and $1/f$ noise voltages. Since sensor signals are typically slow and weak, high-accuracy, high-precision CMOS interfaces usually employ dynamic techniques for compensating both the input offset and $1/f$ noise voltages of opamps [5]–[11].

An additional issue arises in submicrometer CMOS circuits, where various obstacles may inhibit the design of feedback amplifiers with high loop gain, which is a prerequisite for achieving a small relative gain error [5]. In fact, first, low supply voltages reduce the dynamic range and make cascode techniques problematic; second, short channel effects reduce the dynamic drain-to-source resistance of MOSFETs. Both of the aforementioned difficulties result in a lower gain per stage; although it would still be possible to make a large loop gain by cascading more amplification stages, the frequency compensation of multistage amplifiers is more problematic and generally results in larger power consumption and chip area. As a result, in deep submicrometer CMOS electronic interfaces, beside the input offset and $1/f$ noise voltages, it may be important to compensate for the finite gain of the opamp; although this can be done with autozero [6], dynamic element matching (DEM) or chopper amplifiers using resistive feedback networks are often preferred in sensor interfaces [5]–[9] as autozeroing results in a higher residual noise due to the undersampled wideband thermal noise [6]. Recently, in order to compensate the finite opamp gain as well as the input offset and $1/f$ noise voltages without undersampling the thermal noise, the dynamic opamp matching technique has been introduced [7], [9], [11]; such a solution is, however, nonoptimal from the point of view of area, power consumption, and residual noise, as it requires two distinct opamps and two feedback networks.

Another important problem in CMOS opamp circuits is the tradeoff between output swing and output resistance; in fact, even if almost always high-accuracy high-precision CMOS amplifiers do not drive significant loads, the output resistance of rail-to-rail CMOS opamps is so poor that resistive feedback networks may already degrade their accuracy (the integration of high feedback resistances is impractical).

Here, we show how to design high-accuracy, high-precision amplifiers by taking advantage of the *current-mode* approach [12]–[14], combined with a proper DEM strategy. In fact, in principle, the application of DEM to a second-generation current conveyor (CCII [4]) allows to compensate for the input offset and $1/f$ noise voltages of the nominally identical (source-coupled) input transistor pairs as well as the error of the output current mirror due to transistor mismatch [15]. The resulting DEM-CCII circuits can be advantageous for the integration of high-accuracy, high-precision CMOS amplifiers; in comparison with autozero circuits, DEM-CCIIs have a lower residual noise; in comparison with traditional chopper or DEM circuits, DEM-CCIIs are less sensitive to the finite opamp gain and can alleviate the tradeoff between output resistance and output swing; in comparison with dynamic opamp matching, DEM-CCIIs are more area- and power-efficient and have a residual rms input equivalent noise voltage which is $\sqrt{2}$ times smaller. DEM-CCIIs are especially suitable for amplification stages before integrating analog-to-digital converters (ADCs); in other applications, an additional low-pass filter may be necessary. It should also be observed that the proposed solution is only suitable if the load driven by the amplifier is negligible, as for other CCII-based amplifiers (this is, however, seldom a problem in integrated CMOS circuits).

Manuscript received July 19, 2007; revised October 10, 2007. This paper was recommended by Associate Editor M. Delgado-Restituto.

C. Falconi and A. D'Amico are with the Department of Electrical Engineering, University of Rome Tor Vergata, Rome, 00130, Italy, and also with CNR IDAC, 00133, Rome, Italy (e-mail: falconi@eln.uniroma2.it).

D. Mazzieri is with the Department of Electrical Engineering, University of Rome Tor Vergata, Rome, 00130, Italy.

G. Ferri, V. Stornelli, and A. De Marcellis are with the Department of Electrical and Information Engineering, University of L'Aquila, Monteluco di Roio—L'Aquila, 67100, Italy.

Digital Object Identifier 10.1109/TCSII.2007.914407

II. Gain Error of CCII Amplifiers

CCIIs are current-mode analog building blocks [4] which have three terminals, conventionally named X, Y, and Z; ideally, if an input voltage is applied to the Y-node, the CCII produces an equal voltage at the X-node (with zero output impedance); furthermore, the current flowing into the X-node is mirrored (equal or opposite) into the Z-node (with infinite output impedance).

In practical implementations, the nonideal impedances at the CCII terminals must be considered. In particular, in typical CCII topologies, the impedance at the X-node (ideally zero) is inversely proportional to the g_m of the input transistors; as a result, a low impedance at the node X requires large values of g_m, so that there is a tradeoff with power consumption. In a similar manner, the impedance at the node Z (ideally infinite) may not be too high due to the finite value of $r_{\rm ds}$ (especially in presence of short channel effects). Obviously, the nonideal impedances at the X- and Z-nodes introduce errors.

Fig. 1(a) and (b) shows, respectively, a traditional opamp noninverting voltage amplifier and the correspondent CCII amplifier; equivalently, the CCII amplifier can be modeled by an opamp voltage buffer and a controlled current source, as shown in Fig. 1(c). Finally, Fig. 1(d) shows the CCII voltage amplifier with the opamp replaced by a Thevenin equivalent circuit. In the following analysis, for the sake of comparison, the open-loop gain of the opamps G_0 is assumed to be the same. Ideally, the voltage gain of the CCII amplifier [shown in Fig. 1(b)] is

$$A_{V,\rm ideal} = \frac{R_2}{R_1}. \tag{1}$$

In the opamp amplifier shown in Fig. 1(a), the loop gain is $G_0R_1/(R_1+R_2)$, while, in the CCII amplifier the loop gain is G_0 (here the opamp is connected as a buffer and the voltage amplification is achieved out of the loop by means of the controlled current source). In standard feedback systems, in order to keep the relative gain error small, the magnitude of the loop gain must be much larger than 1; however, this condition is far less stringent for the amplifier in Fig. 1(b) (especially if $(R_1+R_2)/R_1$ is large). By inspection of Fig. 1(d), we find

$$\begin{aligned} i_{\rm out} &= \frac{G_0}{R_1 + R_{\rm out,1} + G_0R_1} v_{\rm in} \\ v_{\rm out} &= \frac{G_0R_{\rm out,2}A_{V,\rm ideal}R_1}{(A_{V,\rm ideal}R_1 + R_{\rm out,2})(R_1 + R_{\rm out,1} + G_0R_1)} v_{\rm in} \end{aligned} \tag{2}$$

so the gain of the CCII amplifier is given by

$$\begin{aligned} A_V &= A_{V,\rm ideal}\frac{R_1G_0}{R_1 + R_{\rm out,1} + G_0R_1} \cdot \frac{R_{\rm out,2}}{A_{V,\rm ideal}R_1 + R_{\rm out,2}} \\ &= A_{V,\rm ideal}(1+\delta_1)(1+\delta_2) \end{aligned} \tag{3}$$

where $A_{V,\rm ideal}$ is the ideal gain [see (1)] and

$$\begin{aligned} \delta_1 &= \frac{-(R_1 + R_{\rm out,1})}{R_1 + R_{\rm out,1} + G_0R_1} \\ \delta_2 &= \frac{-R_2}{R_2 + R_{\rm out,2}}. \end{aligned} \tag{4}$$

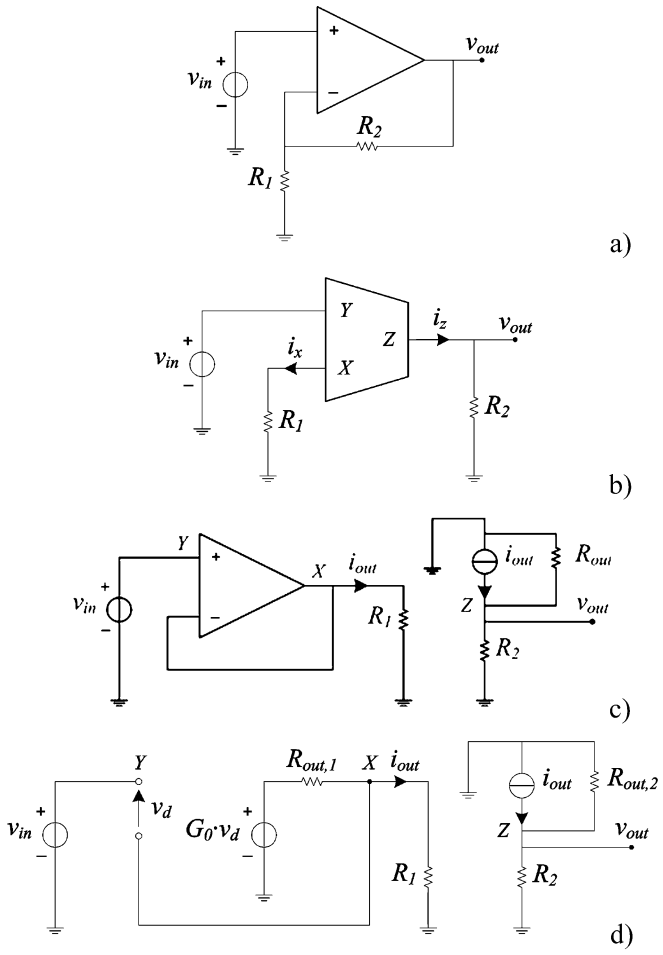

Fig. 1. (a) Opamp noninverting voltage amplifier. (b) CCII noninverting voltage amplifier. (c) CCII noninverting voltage amplifier where the CCII is represented by a unity-feedback opamp and a controlled current source. (d) CCII noninverting voltage amplifier with a Thevenin equivalent circuit for the unity-feedback opamp.

Clearly, our goal is to make the gain A_V as close as possible to the ideal gain $A_{V,\rm ideal}$. Since the two terms δ_1 and δ_2 are both negative, they may not compensate each other and, therefore, should be reduced as much as possible. In particular, imposing $|\delta_1| << 1$ and $|\delta_2| << 1$ corresponds to the following design conditions for the CCII:

$$\begin{cases} G_0R_1 >> R_1 + R_{\rm out,1} \\ R_{\rm out,2} >> R_2. \end{cases} \tag{5}$$

Once these conditions are satisfied, the gain A_V may be simplified as follows:

$$A_V \cong A_{V,\rm ideal} + A_{V,\rm ideal}(\delta_1 + \delta_2) \tag{6}$$

so that the gain error GE and the relative gain error RGE are

$$\begin{aligned} {\rm GE_{CCII}} &= A_V - A_{V,\rm ideal} \\ &= A_{V,\rm ideal}(\delta_1 + \delta_2), \\ {\rm RGE_{CCII}} &= \frac{A_V - A_{V,\rm ideal}}{A_{V,\rm ideal}} = \delta_1 + \delta_2. \end{aligned} \tag{7}$$

In the aforementioned analysis, the error of the current mirror which mirrors the current $i_{\rm out}$ from X to the Z-node of the CCII has been neglected; in practice, this error can be made negligible by a proper application of the DEM technique (using cascode topologies, the RGE of well-designed current mirrors after DEM may be of the order of 0.1%). For the opamp-based amplifier with negligible load, we find

$$A_{V,\rm ideal} = \frac{R_1+R_2}{R_1}$$
$$A_V = \frac{G_0(R_1+R_2)}{(1+G_0)R_1+R_2+R_{\rm out}}$$
$$\mathrm{RGE_{OA}} = \frac{-(R_1+R_2+R_{\rm out})}{(1+G_0)R_1+R_2+R_{\rm out}} \quad (8)$$

where $R_{\rm out}$ is the opamp output resistance. Comparing (7) and (8), it is evident that, besides a large gain G_0, achieving a low RGE also requires small values of, respectively, $R_{\rm out,1}$ and $R_{\rm out}$; this is, however, more critical in opamp amplifiers because low-output resistance stages (e.g., common drain) can only be used decreasing the output swing (by contrast, in the CCII amplifier, $R_{\rm out,1}$ is the dynamic resistance of an *internal* node and, in principle, can be made low without reducing the output swing). In practice, if G_0 is sufficiently large and both $R_{\rm out}$ and $R_{\rm out,1}$ are sufficiently enough (these conditions are necessary prerequisites for low RGE), the term δ_1 [see (4) and (7)] is about R_2/R_1 times smaller than $\mathrm{RGE_{OA}}$; as a result, $\mathrm{RGE_{CCII}}$ is also about R_2/R_1 times smaller than $\mathrm{RGE_{OA}}$, provided that the term δ_2 is made negligible by making $R_{\rm out,2}$ sufficiently larger than R_2. Depending on the process and the resistance R_2, in some cases the term δ_2 could be made negligible by simply using long-channel devices in a rail-to-rail output stage (e.g., common source); in other cases, especially in deep submicrometer processes, a cascode output stage could be necessary; clearly, although both these possibilities somehow limit the output swing, the CCII-based amplifier will still perform better than the correspondent opamp amplifier. In conclusion, achieving a low RGE requires a high output resistance for CCII amplifiers; in low-voltage, deep submicrometer CMOS systems, this is clearly a decisive advantage over opamp circuits that can only achieve a low RGE if their output resistance is sufficiently low (a requirement that is in contrast with output swing specifications).

As an example, assuming both $R_{\rm out}$ and $R_{\rm out,1}$ are equal to zero (as previously discussed, this is more critical for opamp circuits) and considering a fixed value for R_1, Fig. 2 shows the RGE of opamp and CCII amplifiers as a function of the open-loop gain G_0 for different values of the ideal voltage gain $A_{V,\rm ideal}$. As evident from Fig. 2, the RGEs of opamp amplifiers are, approximately, inversely proportional to G_0 and directly proportional to their ideal voltage gain $(R_1+R_2)/R_1$; by contrast, the RGE of CCII amplifiers is dominated by δ_1 (approximately inversely proportional to G_0 and independent of $A_{V,\rm ideal}$) for low values of G_0 and by δ_2 (independent of G_0 and approximately proportional to R_2 if the obvious condition $R_{\rm out,2} \gg R_2$ is satisfied) for high values of G_0.

In conclusion, for not so high values of G_0 (e.g., deep submicrometer CMOS circuits), the CCII as preferable as their RGE, dominated by the term δ_1, is about R_2/R_1 times smaller than $\mathrm{RGE_{OA}}$. We, however, stress that in our analysis we have not considered an intrinsic limit for both the opamp and the CCII amplifiers, namely the error in the ratio between R_2 and R_1; however, with proper layout, the contribution of this error to the RGE can be of the order of 0.001.

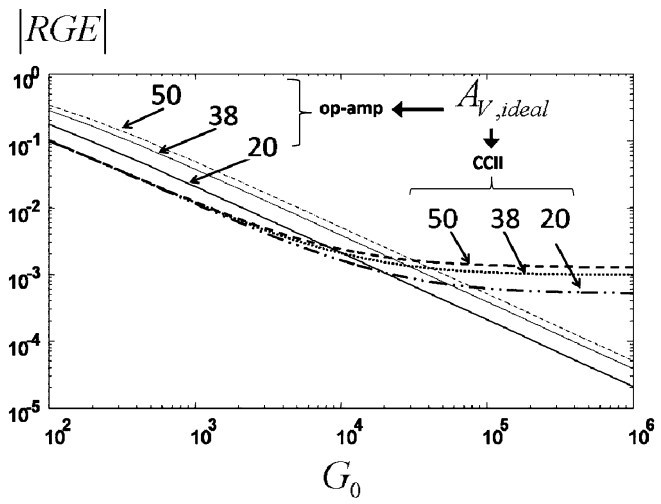

Fig. 2. | RGE | for CCII and opamp amplifiers. For all of the simulations, $R_1 = 50\Omega, R_{\rm out} = R_{\rm out,1} = 0\Omega, R_{\rm out,2} = 2$ MΩ. CCII: $R_2 = 2.5$ kΩ ($A_{V,\rm ideal} = 50$); $R_2 = 1.9$ kΩ ($A_{V,\rm ideal} = 38$); $R_2 = 1000\Omega$ ($A_{V,\rm ideal} = 20$). Opamp: $R_2 = 2.45$ kΩ ($A_{V,\rm ideal} = 50$), $R_2 = 1.85$ kΩ ($A_{V,\rm ideal} = 38$), $R_2 = 950\Omega$ ($A_{V,\rm ideal} = 20$).

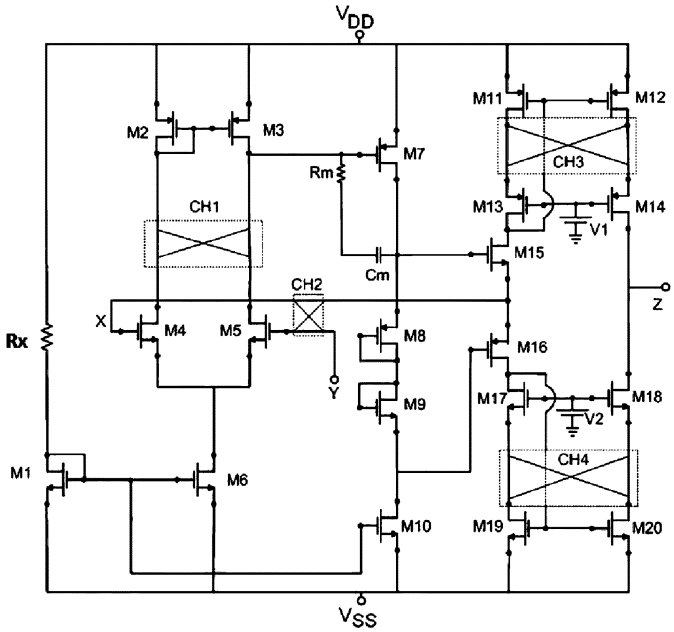

Fig. 3. Proposed Miller-compensated DEM-CCII.

III. DEM-CCII

Based on our analysis, we have designed, in a standard CMOS process (AMS 0.35 μm), the DEM-CCII shown in Fig. 3. The CCII is based on a two-stage Miller-compensated OTA with a class-AB output stage and a low-voltage cascode current mirror for injecting the output current of the buffer-connected OTA into the Z-node. In fact, since the errors of the output current mirror increase the overall RGE [see the term δ_2 as expressed in (4)], a high impedance is required. In

TABLE I
MAIN CHARACTERISTICS OF THE DEM-CCII (FIG. 3)

Parameter	Value
Voltage supply	±1.65 *V*
Power consumption	309μW
Open loop voltage gain (op amp)	3990
Slew Rate	13.5 $V/\mu s$
Z node Resistance	5.4 $M\Omega$
X node Resistance	107 $m\Omega$ ($=R_{out,1}/G_0$)
Systematic input offset voltage	43μV
Chopper clock frequency	100 *kHz*
Output swing	up:+1.19*V*; down:-1.14*V*

practice, the output resistance should be so large that the term δ_2 in (7) becomes negligible; under these conditions, besides alleviating the tradeoff between output resistance and output swing, $\mathrm{RGE_{CCII}}$ will be about R_2/R_1 times smaller than $\mathrm{RGE_{OA}}$. In order to compensate for both the input offset and $1/f$ noise voltages, the DEM technique is applied by means of the chopper switches $\mathrm{CH_1}$–$\mathrm{CH_4}$ so that all of the critical transistor pairs [$(M2, M3)$, $(M4, M5)$, $(M11, M12)$, and $(M19, M20)$] are dynamically matched; since the transistors implementing the output current mirror are outside the loop, it is also mandatory to compensate for their mismatch (chopper switches $\mathrm{CH_3}$ and $\mathrm{CH_4}$); in practice, the chopper switches also reduce the low-frequency distortion which, in current-mode circuits, is often dominated by threshold voltage mismatch [14].

The dc gain of the opamp inside the CCII is around 4000; the Miller capacitor C_M is equal to 50 pF, while the resistor R_M, which removes the right half-plane zero, is equal to 12 kΩ; the main characteristics of this CCII are reported in Table I. As expected, the input equivalent noise *before* DEM contains a significant $1/f$ contribution (about 170 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$@1 kHz); however, since this noise is mainly due to the input transistors, DEM with a frequency higher than the corner frequency removes the $1/f$ noise (the analytical expressions for the residual noise are the same as those for chopper circuits in [6]). In order to perform preliminary tests, the mismatch between nominally identical transistors has been modeled by means of auxiliary voltage sources in series with the gates of mismatched devices. Though in many interfaces the amplifier can be followed by an integrating ADC, in other applications the output ripple must be filtered; in these cases, in comparison with chopper circuits, the proposed solution may require an additional low-pass filter as the ripple due to the mismatch between the transistors of the output current mirror is not filtered by the (Miller-multiplied) capacitor C_M. In order to not excessively increase the chip area, this filter could be integrated using a capacitance multiplier (e.g., see [4, p. 152]).

Fig. 4 shows a transient analysis when a voltage step of 500 μV is applied at the Y-node [see Fig. 4(a)]. The mismatch between $M4 - M5$ and $M11 - M12$ has been simulated by means of auxiliary 500-μV dc voltage sources in series with the gates of $M5$ and $M12$. The output (node Z) error of the amplifier is shown in Fig. 4(b); the input equivalent error is

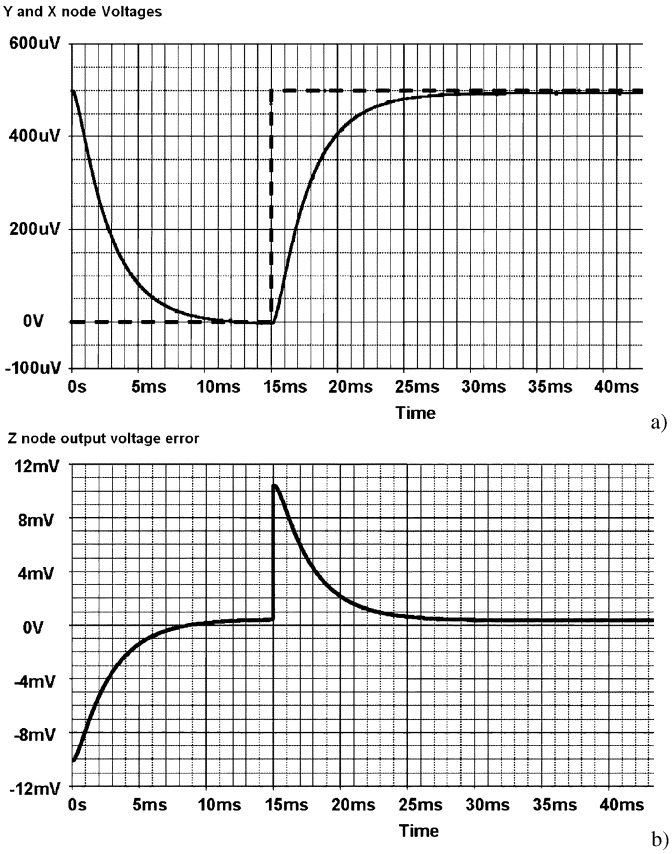

Fig. 4. Step (500 μV) response of the CCII-DEM ($R_1 = 50\Omega$ and $R_2 = 1.9$ kΩ) with an auxiliary low-pass filter. Mismatch between $M4 - M5$ and $M11 - M12$ has been simulated by means of auxiliary dc voltage sources equal to 500 μV. (a) Y-node (dashed line) and X-node (solid line) voltages. (b) Output voltage error at Z-node.

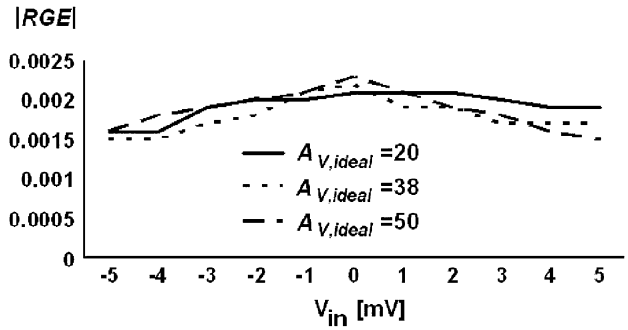

Fig. 5. | RGE | for the CMOS DEM-CCII amplifier as a function of the input voltage.

therefore only a few microvolts (for clarity, a low-pass filter with a cutoff frequency of a few hertz has been added).

Fig. 5 shows the simulated RGEs for three different values of the ideal voltage gain as a function of the input voltage. Obviously, DEM only compensates for the input offset and $1/f$ noise voltages and should not affect the gain error; in fact, the values reported in Fig. 5 have been obtained *after* DEM and include the error of the output current mirror in the CCII. Finally, Fig. 6 shows the theoretical values of $\mathrm{RGE_{CCII}}$, δ_1, and δ_2 for the proposed CMOS CCII amplifier (see (4), (7), Fig. 3, and Table I) as a function of R_2; according to our discussion, since $R_{\mathrm{out},2}$ is

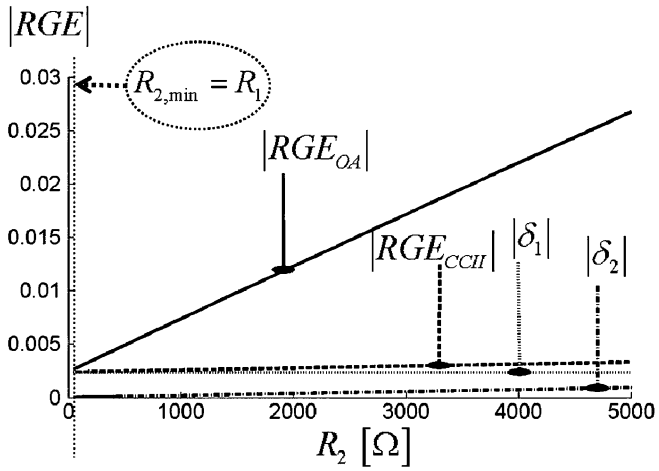

Fig. 6. | RGE | for opamp and CCII amplifiers as a function of R_2. For all the simulations, $R_1 = 50\ \Omega, R_{\rm out} = R_{\rm out,1} = 107\ \mathrm{m}\Omega, R_{\rm out,2} = 5.4\ \mathrm{M}\Omega, G_0 = 3990$.

always much larger than R_2, the term δ_2 is very small and only slightly increases as R_2 increases; the term δ_1 does not depend on R_2. For comparison, Fig. 6 also shows $\mathrm{RGE_{OA}}$ for an opamp amplifier using the opamp included in the CCII. As previously discussed, since δ_2 is very small, $\mathrm{RGE_{OA}}$ is about R_2/R_1 times bigger than $\mathrm{RGE_{CCII}}$ (so that $\mathrm{RGE_{OA}}$ is approximately equal to $\mathrm{RGE_{CCII}}$ if $R_2 = R_1$).

IV. Conclusion

We have applied the DEM technique for compensating the input offset and $1/f$ noise voltages of a CMOS CCII voltage amplifier. In comparison with classic opamp solutions, the gain error may be smaller, as demonstrated both in an analytical manner and through simulations. As an additional decisive advantage over correspondent opamp circuits, the proposed approach can alleviate the tradeoff between output swing and output resistance; in fact, for low RGE, the output resistance seen at the output node (i.e., where there is voltage gain) must be very high for CCII amplifiers and very low for opamp amplifiers. The resulting circuits, DEM-CCIIs, are especially suitable for amplification stages before integrating ADCs; in other applications, since the mismatch between transistors of the output current mirror must also be compensated, the Miller capacitor inside the opamp is not sufficient for filtering the output ripple, and an additional low-pass filter can be required.

References

[1] R. Hogervorst and J. Huijsing, *Design of Low-Voltage Low-Power Operational Amplifier Cells*. Boston, MA: Kluwer, 1996.
[2] W. A. Serdijn, A. C. Vander Woerd, and J. C. Kuenen, *Low-Voltage Low-Power Analog Integrated Circuits*. Boston, MA: Kluwer, 1995.
[3] S. Sakurai and M. Ismail, *Low-Voltage CMOS Operational Amplifiers*. Boston, MA: Kluwer, 1995.
[4] G. Ferri and N. Guerrini, *Low voltage Low Power CMOS Current Conveyors*. Boston, MA: Kluwer, 2003.
[5] C. Falconi, E. Martinelli, C. Di Natale, A. D'Amico, F. Maloberti, P. Malcovati, A. Baschirotto, V. Stornelli, and G. Ferri, "Electronic interfaces," *Sens. Act. B*, vol. 121, pp. 295–329, 2007.
[6] C. Enz and G. Temes, "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling and chopper stabilization," *Proc. IEEE*, vol. 84, no. 11, pp. 1584–1613, Nov. 1996.
[7] C. Falconi, C. Di Natale, A. D'Amico, and M. Faccio, "Electronic interface for the accurate read-out of resistive sensors in low voltage-low power integrated systems," *Sens. Act. A*, vol. 117, pp. 121–126, 2005.
[8] J. F. Witte, K. A. Makinwa, and J. H. Huijsing, "A CMOS chopper offset-stabilized opamp," in *Proc. IEEE ESSCIRC*, 2006, vol. 1, pp. 360–363.
[9] C. Falconi, A. D'Amico, and M. Faccio, "Design of accurate analog circuits for low voltage low power CMOS systems," in *Proc. IEEE ISCAS*, 2003, vol. 1, pp. 429–432.
[10] R. J. van de Plassche, "Dynamic element matching for high accuracy monolithic D/A converters," *IEEE J. Solid-State Circuits*, vol. SC-11, no. 3, pp. 795–800, Jun. 1976.
[11] C. Falconi, C. Di Natale, and A. D'Amico, "Dynamic op amp matching: A new approach to the design of accurate electronic interfaces for low voltage/low power integrated sensors systems," in *Proc. Eurosensors*, Prague, Czech Republic, pp. 539–540.
[12] C. Toumazou, A. Payne, and D. Haigh, *Analogue IC Design: The Current Mode Approach*. London, U.K.: Peter Peregrinus, 1990.
[13] G. Palumbo, S. Palmisano, and S. Pennisi, *CMOS Current Amplifiers*. Boston, MA: Kluwer, 1999.
[14] K. Koli and K. Halonen, *CMOS Current Amplifiers*. Boston, MA: Kluwer, 2002.
[15] V. Stornelli, G. Ferri, A. De Marcellis, C. Falconi, D. Mazzieri, and A. D. Amico, "High-accuracy, high-precision DEM-CCII amplifiers," in *Proc. IEEE ISCAS*, May 2007, pp. 2196–2199.