High Light-Load Efficiency Charge Pumps

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***Abstract*—Here, first, we analyze the undesired charge transfer occurring in charge pumps; afterwards we present a circuit which is less susceptible to this issue, resulting in significant improvements of the light load efficiency in charge pumps which must have a sufficiently high maximum current capability. SPICE simulations confirm the theoretical results.**

I. INTRODUCTION

The continuous trend toward portable, low voltage, battery-powered, and fully integrated systems make charge pumps essential building blocks for analog and mixed-mode circuits [1-3]. In many battery-powered systems the autonomy is limited by the power consumption occurring at light-load; in these conditions, an important source of power losses is the undesired charge transfer.

Here, first, we discuss the origin of the undesired charge transfer in CMOS charge pumps and we give simple conditions for verifying if the problem is present in a given charge pump; afterwards we present a new circuit which keeps the undesired charge transfer at a very low level, thus improving the light-load efficiency. The proposed charge pump has been designed in a standard $1.6\mu m$ CMOS process and compared with existing circuits.

II. UNDESIRED CHARGE TRANSFER IN CHARGE PUMPS

It is well known [4-6] that undesired charge transfer in charge pumps may degrade efficiency. Since the timing of the control signals is critical in determining the undesired charge transfer, it is useful to introduce the following definitions.

If the signal a is a voltage square waveform, we refer to its transitions from the low level to the high level with the symbol $a(L \to H)$ and to its transitions from the high level to the low level with $a(H \to L)$.

For two given anti-phase control signals (a_1, a_2),

- if there are time periods when both (a_1, a_2) are low, we say that they are *OV_L* ;
- if there are time periods when both (a_1, a_2) are high, we say that they are *OV_H*;
- if there are no periods when (a_1, a_2) are simultaneously low or high, since their rise and fall times may not be zero, their transitions must overlap and we say that they are *OV_T*.

Let us now consider the classic CMOS voltage doubler shown in fig. 1 [5]; in this circuit (a_1, a_2) are anti-phase clock signals which swing from *0* to V_{DD}. Transistors M_5 and M_6 generate the auxiliary voltage for preventing forward-biasing of the pn junctions constituted by the n-well and the adjacent p-type regions [5]; in other words M_5 and M_6 bias the n-well (where all the PMOS transistors of the charge pumps are fabricated). If (a_1, a_2) are *OV_H* and, immediately after $a_1(0 \to 1)$, the signal a_2 is still high, both M_1 and M_2 are on; M_1 will then short V_{DD} and a_{11}, which has been raised toward $2V_{DD}$ by the transition $a_1(0 \to 1)$, so that an undesired charge transfer will result. If, on the contrary, (a_1, a_2) are *OV_L,* the dual problem is found for the PMOS transistors M_3 and M_4. If (a_1, a_2) are *OV_T*, an undesired charge transfer will occur during the *overlapping transitions* of a_1 and a_2. Similar problems are found in other charge pumps. Obviously, for a given circuit topology and a given timing of the control signals, the larger the width of the transistors, the larger the undesired charge transfer; the difficulty is serious in systems where high light-load efficiency is essential, as in those conditions even small power losses may be critical.

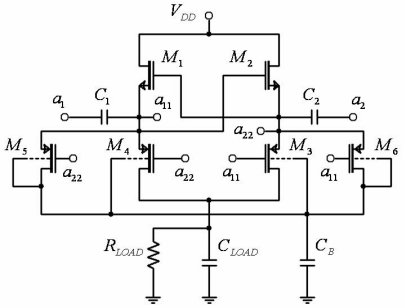

Figure 1. CP1: classic voltage doubler [5].

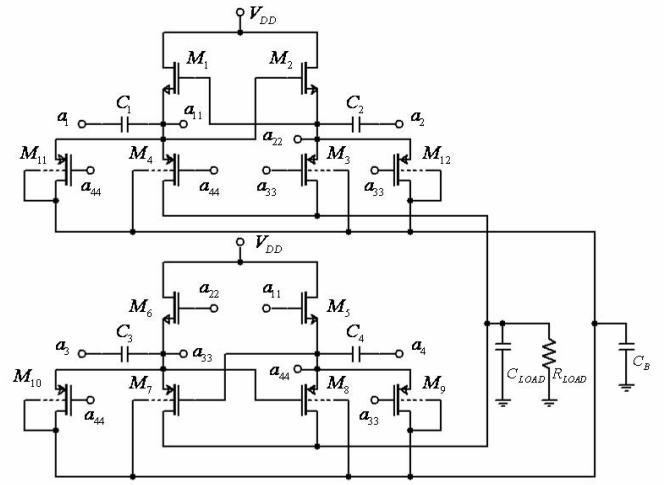

Figure 2. CP2: charge pump with reduced undesired charge transfer [4].

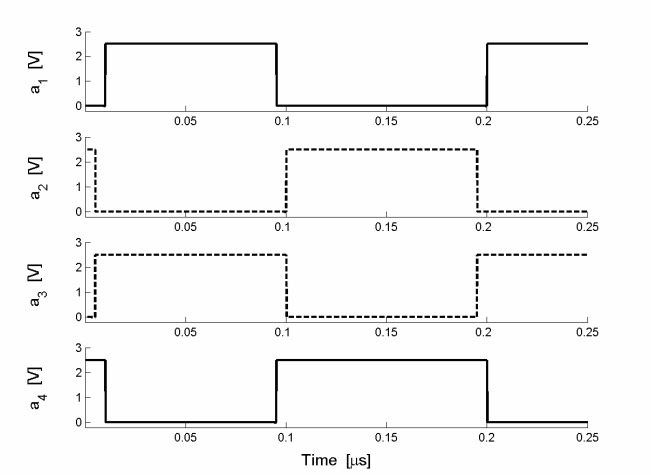

Figure 3. Control signals for the circuit in fig. 2.

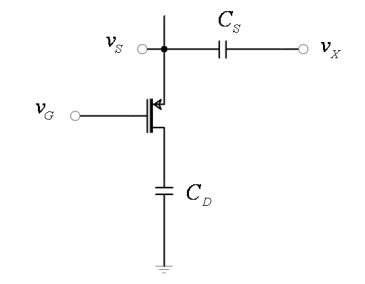

Figure 4. PMOS transistor in a charge pump.

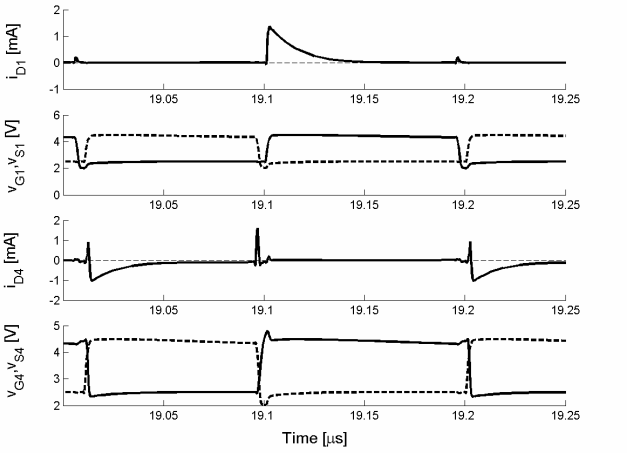

Figure 5. Simulated signals in the circuit in fig. 2.

A first solution has been proposed in [4] (see the circuit shown in fig. 2), where transistors M_9, M_{10}, M_{11} and M_{12} bias the n-well; control signals are shown in fig. 3. The undesired charge transfer is reduced, but not completely solved [4], as explained below.

Let us consider the PMOS transistor shown in fig. 4 (which is representative of PMOS transistors in the charge pump); the drain voltage is $2V_{DD}$. If the transistor is on and we want to switch it off, we must make sure that $v_G(L \to H)$ before the source voltage is changed (otherwise, if the transistor is still on even after the source voltage has already been changed, undesired charge transfer will occur). Similar considerations apply to the opposite transitions and for NMOS transistors. In summary:

a) if a transistor (NMOS or PMOS) must be switched from on to off, its gate voltage must be (accordingly) changed *before* its source voltage is changed;

b) if a transistor (NMOS or PMOS) must be switched from off to on, its gate voltage must be (accordingly) changed *after* its source voltage is changed.

These conditions are equivalent to the following one (much easier to be verified): the gate and the source voltages of NMOS transistors must be *OV_L*, whereas the gate and the source voltages of PMOS transistors must be *OV_H*. The previous analysis neglects the time for switching on and off the transistors and the parasitic capacitive paths to the bulk; however, generally, these effects give smaller contributions.

As to the circuit [4] (fig. 2), there is no undesired charge transfer in (M_1,M_2,M_7,M_8), but there is undesired charge transfer in (M_3,M_4,M_5,M_6); this analysis is confirmed by simulations in fig. 5 (the current i_{D4} should always be *negative* as currents are considered positive when they enter the terminal).

III. CHARGE PUMP LESS SUSCEPTIBLE TO UNDESIRED CHARGE TRANSFER

Fig. 6 shows the proposed circuit; the transistors M_{33} and M_{44} are used for generating the signals (p_3, p_4); M_5 and M_6 bias the n-well. If the control signals depicted in fig. 7 are used, the conditions above discussed are satisfied for all transistors but M_{33} and M_{44}, which however may be very small (resulting in very little power losses). Fig. 8 confirms that the undesired charge transfer is greatly reduced.

In order to test the proposed solution, three fully integrated charge pumps have been designed in a standard $1.6\mu m$ CMOS process. In the first charge pump (fig. 1), the control signals (a_1, a_2) are OV_T (different conditions may easily lead to an even lower efficiency). In comparison with the classic voltage doubler, both the second circuit (fig. 2) and the third circuit (fig. 6) are expected to have a better light-load efficiency and an higher final output voltage (since undesired charge transfer also reduces the final output voltage). In all of the following simulations, a single parameter is changed while all the other parameters are set at their *reference value* (see table I). The three charge pumps have the same total area.

Fig. 9 shows the efficiency and the final output voltage as a function of the load resistance; the efficiency improvement is, clearly, more evident under light-load conditions.

Fig. 10 shows the efficiency and the final output voltage as a function of the width of the NMOS transistors (the width of the PMOS transistors has been changed according to $w_p = 2.3 w_n$). Efficiency improvements are obtained only if the width of the transistors is sufficiently large (as this exacerbates the undesired charge transfer issue).

Fig. 11 shows the efficiency and the final output voltage as a function of the frequency of the control signals.

Fig. 12 shows the efficiency and the final output voltage as a function of the supply voltage; all the charge pumps may be used in low voltage applications; if a more recent process (lower threshold voltages) is used, the minimum operating voltage of the charge pumps would be significantly lower.

IV. CONCLUSIONS

We have given conditions for determining if undesired charge transfer occurs in a given charge pump. These conditions may be used for designing new circuits less susceptible to this problem; as an example, a new charge pump has been proposed. In comparison with existing solutions, the additional circuit complexity is minimal; although a more complex timing strategy is necessary, the new charge pump offers both an higher final output voltage and a better efficiency if the transistor widths are enough large (see figure 10). At light load, the efficiency of the proposed circuit is much higher than the efficiency of classic circuit, thus significantly extending the battery lifetime (see the efficiency for large load resistors in fig. 9).

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TABLE I.

Reference parameters for the charge pumps CP1, CP2, CP3			
Parameter	***CP 1 (fig. 1)***	***CP 2 (fig. 2)***	***CP 3 (fig. 6)***
$w_n^{(a)}$	$300\mu m$	$150\mu m$	$300\mu m$
$w_p^{(b)}$	$690\mu m$	$345\mu m$	$690\mu m$
$w_{n,33}$, $w_{n,44}$	–	–	$2\mu m$
L (for all transistors)	$1.6\mu m$	$1.6\mu m$	$1.6\mu m$
C (pumping capacitors)	$80pF$	$40pF$	$75pF$
C_{33}, C_{44}	–	–	$5pF$
C_{LOAD}	$80pF$	$80pF$	$80pF$
R_{LOAD}	$40k\Omega$	$40k\Omega$	$40k\Omega$
f	$5.3MHz$	$5.3MHz$	$5.3MHz$
V_{DD}	$2.5V$	$2.5V$	$2.5V$
$w_{p,BNW}$ (n-well bias)	$10\mu m$	$5\mu m$	$10\mu m$
C_{BNW} (n-well bias)	$5pF$	$5pF$	$5pF$

a. width of all the N-MOSFETs but those which are separately specified
b. width of all the P-MOSFETs but those which are separately specified

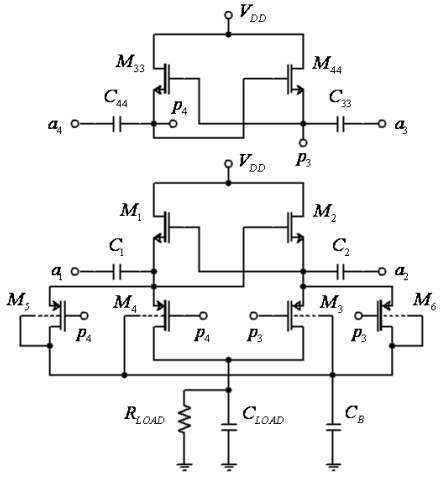

Figure 6. CP3: proposed charge pump.

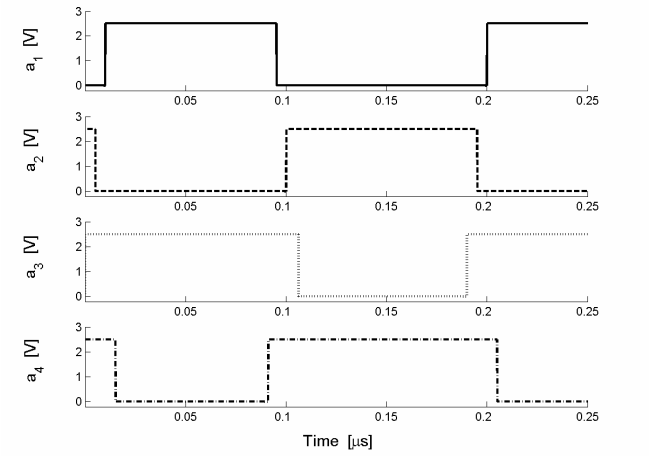

Figure 7. Control signals for the circuit in fig. 6.

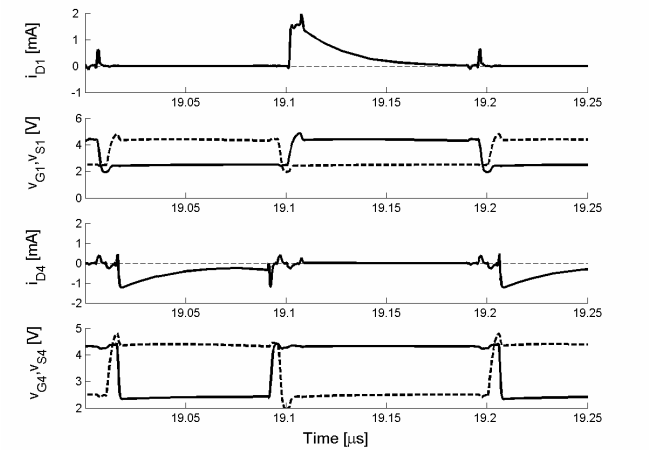

Figure 8. Simulated signals in the circuit in fig. 6.

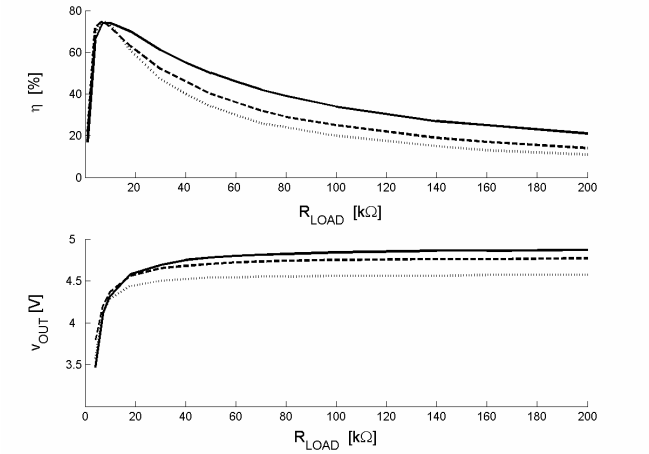

Figure 9. Efficiency and final output voltage of CP1 (dotted line), CP2 (dashed line), CP3 (solid line) vs. the load resistance R_{LOAD}.

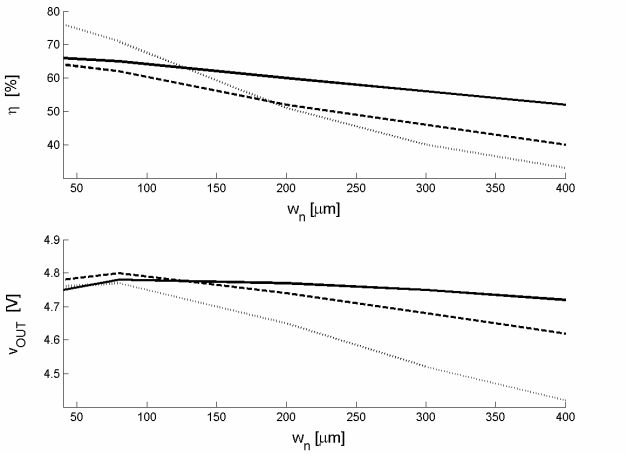

Figure 10. Efficiency and final output voltage of CP1 (dotted line), CP2 (dashed line), CP3 (solid line) vs. the transistor widths.

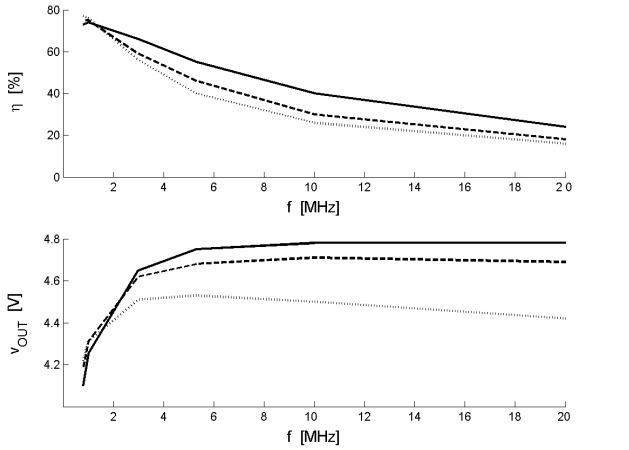

Figure 11. Efficiency and final output voltage of CP1 (dotted line), CP2 (dashed line), CP3 (solid line) vs. the operating frequency *f*.

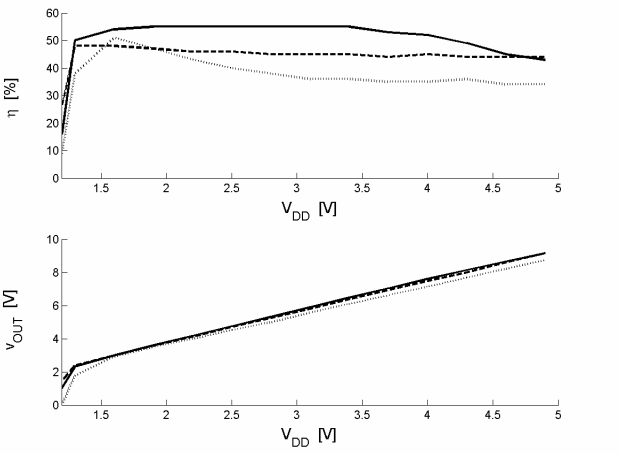

Figure 12. Efficiency and final output voltage of CP1 (dotted line), CP2 (dashed line), CP3 (solid line) vs. the supply voltage V_{DD}.