Op Amp Tuning for High Accuracy Deep Sub-Micron CMOS Analog Circuits

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***Abstract*—As the minimum feature size shrinks, it becomes more and more difficult to design high accuracy CMOS analog circuits. Here we show that circuits using multiple op amps may be significantly more accurate than their traditional counterparts, especially if op amps are properly "tuned".**

I. INTRODUCTION

A powerful method for implementing high accuracy analog circuits is feedback; feedback allows, *if there is enough loop gain,* to relate the accuracy of the closed loop system to the accuracy of the feedback network, instead of to the accuracy of parameters of active devices. Although feedback may introduce stability issues, it is very effective (op amp circuits are the most popular example [1]).

In sub-micron CMOS circuits various obstacles often inhibit the design of amplifiers with *enough loop gain*. First, low supply voltages make cascode techniques problematic; second, short channel effects reduce the output resistance of MOSFETs. Both the aforementioned difficulties result in a lower gain per stage; if the gain per stage is limited, it is still possible to make a large loop gain by cascading more amplification stages. Multistage amplifiers also have some disadvantages, the first being a more problematic frequency compensation; for this reason many *ad hoc* frequency compensation techniques have been proposed for CMOS multistage amplifiers [2-4]. There is, however, still a need to develop solutions for high accuracy CMOS analog circuits. Here a possible approach is described.

Instead of one operational amplifier, more operational amplifiers may be used so that their combination makes the circuit more accurate. In other words, many (relatively) "poor" op amps cooperate for producing an accurate output signal. This idea is very old and has been named *composite amplifier* [5,6]. Traditionally, these circuits were used for merging the good qualities of two *different* op amps; as an example, a proper combination of an ultra-fast op amp and of a low-offset op amp may result in the same accuracy given by an hypothetic ultra-fast, low-offset op amp.

The need for high accuracy analog CMOS circuits led to a different application of the same idea: two (nominally) *identical* op amps implement a single, more accurate, amplifier. The *replica amplifier* circuit proposed in [7,8] compensates the finite op amp gain (gain enhancement); the gain enhancement was limited by "op amp mismatch"; furthermore the circuits [7,8] could not compensate the input offset voltages, even if they were matched (although this is not usually the case, the importance of this aspect will appear later). Recently we have proposed circuits [9-15] which employ two (nominally) *identical* operational amplifiers for compensating both the finite op amp gain and (matched) input offset voltages; furthermore we have shown that "op amp mismatch" can be effectively compensated by applying the well known dynamic element matching to the entire op amps. The resulting technique, "dynamic op amp matching", is presently the best solution for the implementation of high accuracy CMOS electronic interfaces *if the input offset and 1/f noise voltages, and also the finite gain of the op amp must be compensated* [10-12]; in fact, chopper and traditional dynamic element matching circuits may not compensate the finite op amp gain [16], while autozero circuits have worse noise performance (the wideband thermal noise is under-sampled [16]). Both dynamic op amp matching and autozero (the other option for *gain enhancement*) require switching, and are therefore only suitable for low frequency systems, (*e.g.* many electronic interfaces for sensors and micro-systems, where compensation of the input offset and *1/f* noise voltages are also critical). Here we suggest that this limit may be removed if the op amp mismatch is reduced by simple tuning strategies. The resulting technique, "op amp tuning", may compensate the finite op amp gain and the input offset voltages (but not the *1/f* noise voltage).

As a practical example, we consider a fully integrated low drop-out regulator (LDO); high performance LDOs are required in CMOS systems for supplying interference sensitive circuits. The effectiveness of op amp tuning can not be simulated without accurate models of both transistor parameters and of their spread. We have therefore imple-

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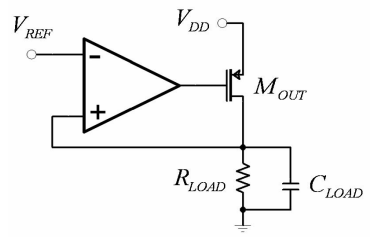

Figure 1. Classic low drop out regulator (LDO).

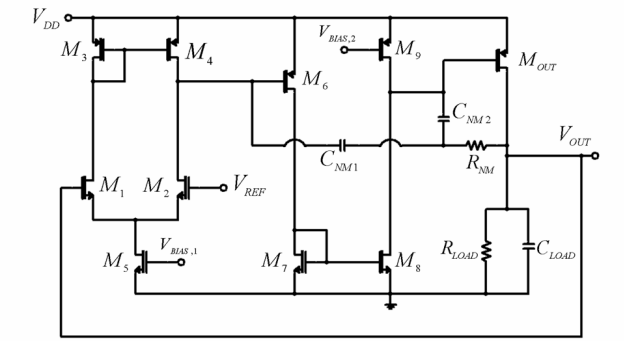

Figure 2. CMOS LDO.

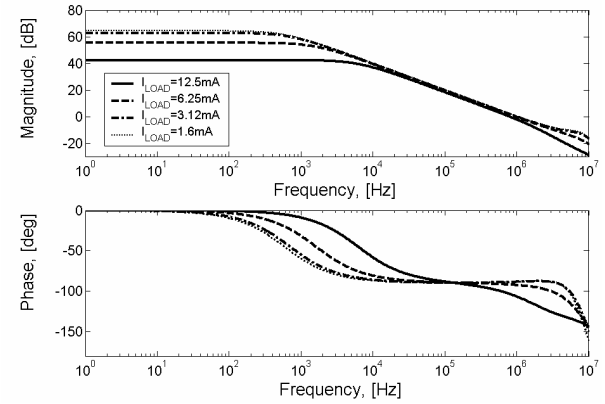

Figure 3. Loop gain of the CMOS LDO shown in fig. 2 for different load currents.

TABLE I.

Parameters of the classic LDO and of the dual op amp LDO			
Parameter	***Value***	***Parameter***	***Value***
$w_{n1} = w_{n2}$	$200\mu m$	R_{LOAD}	$>180\Omega$
w_{n5}	$80\mu m$	C_{LOAD}	$100\,pF$
$w_{n6} = w_{n7} = w_{n8}$	$20\mu m$	C_{NM1}	$20\,pF$
$w_{p3} = w_{p4}$	$40\mu m$	C_{NM2}	$0.5\,pF$
w_{p9}	$40\mu m$	R_{NM}	500Ω
w_{OUT}	$1mm$	n	10
L *(all transistors)*	$2\mu m$	I_{DS5}	$40\mu A$
$R_{C1} = R_{C2}$	$10k\Omega$	I_{SD9}	$10\mu A$

mented a suitable model, reported in [17], in a standard SPICE software. Unfortunately the model given in [17] is relative to an "old" $2\mu m$ process; it is however enough for preliminary tests, which confirm that op amp tuning and advanced frequency compensation techniques may be combined for improving load and line regulation by orders of magnitude.

II. Low Drop-Out Regulators for Deep Sub-Micron CMOS Systems

A. CMOS LDO

Fig. 1 shows the classic low drop-out regulator (LDO). The standard $2\mu m$ CMOS process [17] is considered. The reference voltage and the supply voltage are, respectively, *2.5V* and *3.3V* (much lower supply voltages can be used with more recent processes). The required maximum load current is *12.5mA* (enough for many system-on-chip applications).

Traditional LDOs use large *off-chip* load capacitors [18,19]; such large capacitors make the pole associated to the output node dominant. However, fully integrated LDOs may not use *off-chip* capacitors; a modified nested Miller compensation [20, 21] allows, first, to make the DC loop gain and the phase margin less dependent on the load resistor and, second, to avoid large *off-chip* load capacitors (the non-dominant pole associated to the output node is pushed toward high frequencies by pole splitting). The modified nested Miller compensation [20] has therefore been utilized for compensating the LDO circuit shown in fig. 2 (see C_{NM1}, C_{NM2}, and R_{NM}). In comparison with [21], since in our case the ideal output voltage is exactly the reference voltage, an NMOS input stage is necessary for low drop-out. The PMOS diode M_3 only slightly increases the drop-out because headroom is, anyhow, consumed by the output transistor M_{OUT} ($V_{SD,OUT} > V_{OV,OUT}$ is required for not reducing the loop gain). Table I summarizes the parameters of the CMOS LDO. Fig. 3 shows the loop gain of the regulator; if the load current approaches the maximum output current, the loop gain is reduced; however for currents below *3mA*, the loop gain is almost independent on load current (as in [20]).

B. CMOS dual op amp LDO

If we consider ideally matched op amps, we may design circuits where the errors introduced by different op amps cancel each other [9-15]; as real op amps will be affected by mismatch, mismatch compensation may be necessary.

Fig. 4 shows the proposed dual op amp LDO; it is constituted by a *main regulator* (*MR*) and by an *auxiliary regulator* (*AR*) which interact by means of the compensation resistors (R_{C1},R_{C2}); circuit analysis (op amps and transistors are replaced by linear models) reveals that the circuit may compensate both the finite loop gain and "matched" input offset voltages, which is essential (see later).

Higher accuracy may only be obtained if the following conditions are satisfied. First, the compensation resistors

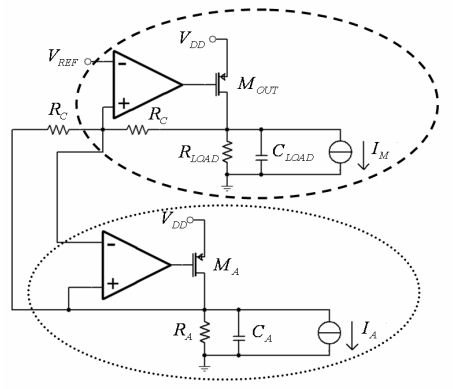

Figure 4. Dual op amp LDO (the *main regulator, MR,* is encircled by a dashed line; the *auxiliary regulator, AR,* is encircled by a dotted line).

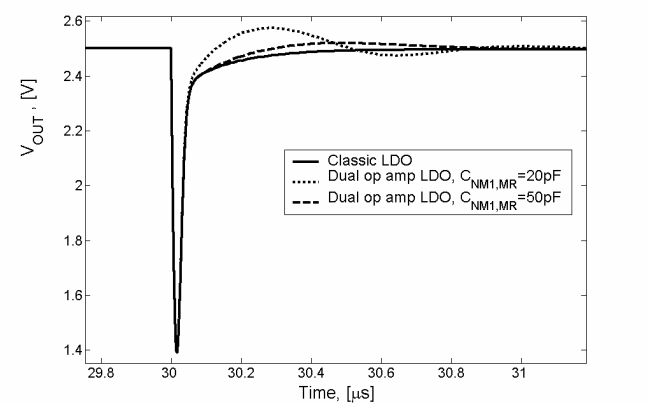

Figure 5. Transient response after a sudden load change.

(R_{C1},R_{C2}) and the op amps should be well matched (the latter is, of course, more problematic). Second, if the width of M_A is n times smaller than the width of M_{OUT}, R_A and C_A must be made, respectively, n times bigger than R_{LOAD} and n times smaller than C_{LOAD} ($n>1$ is important for power efficiency; the condition on capacitors is far less important as the pole associated with C_A is non-dominant). Conditions on load and auxiliary resistors would be impractical in many LDOs (where the *off-chip* load is often unpredictable), but acceptable in many system-on-chip solutions (where the load is *on-chip*). The current sources (I_M,I_A) are necessary if proper operation must be guaranteed even when the load resistor (and accordingly, the auxiliary resistor) are very large; in these conditions, a DC path must be provided for the currents which flow on the compensation resistors (R_{C1},R_{C2}) due to various offset sources; this is not an issue as those currents are so small that very low currents suffice (much smaller than the quiescent current of the regulator). For the CMOS implementation, beside the modifications (according to the previous discussion) due to the choice *n=10,* two identical LDO regulators are used as the *main regulator* and as the *auxiliary regulator* (the circuit and the parameters of each regulator are shown in fig. 2 and table I).

As to stability, the analysis of the multiple loop system shows that, at frequencies where $|A|>>1$, the equivalent loop gain is approximately the same as that of a single regulator, *A*. This demonstrates that, even if the closed loop accuracy is greatly improved, the system is not prone to instability. Transient analysis, however, shows some ringing due to second order effects; ringing may be eliminated if the *main regulator* is made enough slower than the *auxiliary regulator* by increasing its compensation capacitor $C_{NM1,MR}$. Fig. 5 illustrates the transient response to a sudden load change in different conditions.

As to line regulation, tuning is required. If we consider the simple regulator shown in fig. 1, we recognize that the op amp and the following gain stage (M_{OUT},R_{LOAD}) may be regarded as a single op amp. With reference to this op amp, a variation of the supply voltage will result in $\Delta V_{off,in}=(\Delta V_{DD}/p)$, where p is the low frequency $PSRR_{VDD}$ of the op amp. In the proposed regulator, if the $PSRR_{VDD}$ of the two op amps (including the additional gain stage) are "matched", they will result in two "matched" variations of their input equivalent offset voltages; such "matched" variations are, however, compensated by the circuit topology (and could not be compensated with a *replica amplifier*). Matching the $PSRR_{VDD}$ of the two op amps (including the additional gain stage) is therefore useful for line regulation. The low frequency $PSRR_{VDD}$ of those op amps is proportional to $(r_{ds2}//r_{sd4})$; in our circuit r_{ds2} is enough smaller than r_{ds4} and therefore dominates $(r_{ds2}//r_{sd4})$; this observations leads to the tuning strategy described next.

C. Tuning and SPICE simulations

First, Monte Carlo analysis is used to generate both *realistic* op amps and an array of *realistic* transistors $(M_{21},M_{22},...,M_{2N})$ *nominally identical* to M_2 (for our simulations N was chosen equal to *50*). First, the line regulation of the circuit using the two *realistic* op amps is calculated (case "before tuning", see later). Afterwards each transistor from the array $(M_{21},M_{22},...,M_{2N})$ is used in the place of M_2 in the *auxiliary regulator*. Our tuning strategy is to choose the transistor from the array $(M_{21},M_{22},...,M_{2N})$ which *minimizes the line regulation*; we verified that this corresponds to match the $PSRR_{VDD}$ of the two op amps including the additional gain stages (in agreement with the previous discussion). Fig. 6 shows the *PSRR* of the classic CMOS regulator (fig. 2) and of the dual op amp LDO in different conditions; from fig. 6 it also appears that the tuning strategy is robust against temperature variations.

As to load regulation (defined as $\partial V_{OUT}/\partial I_{LOAD}$ [17]), it is largely improved, as expected by circuit analysis. SPICE simulations show that these improvements are good even before tuning, as shown in fig. 7. As a result, first, if only load regulation needs to be improved, it is enough to use the dual op amp LDO and tuning is unnecessary; second, if line regulation is also important, tuning must be finalized to improving the line regulation (as we have done).

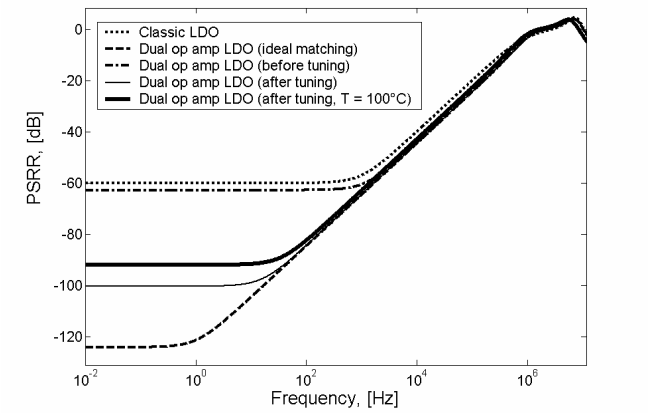

Figure 6. PSRR of the different LDO regulators.

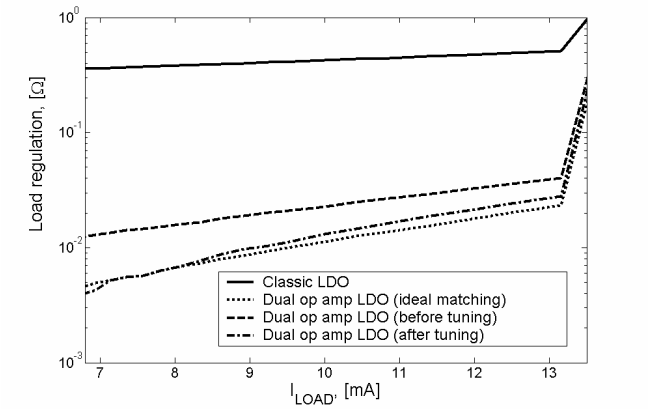

Figure 7. Load regulation of the different LDO regulators.

More *area efficient* strategies can be found (*e.g.* using an array of small transistors to be placed in parallel with M_2); in principle, automatic tuning could be implemented.

III. CONCLUSIONS

In comparison with the classic LDO, the proposed circuit is somewhat slower (see fig. 5) ; this is the cost for large improvements of both load regulation (even without tuning) and line regulation (tuning is required). The presence of two op amps results in larger output noise (approximately, the *rms* output noise voltage is increased by a factor $\sqrt{2}$). As to power consumption, at very light load, when the quiescent currents dominate, power consumption is approximately doubled; if the load current dominates and the ratio n is enough large, power consumption is only slightly increased. The chip area occupied by the dual op amp LDO would not be significantly increased if the area is dominated by the power transistor and the ratio n is enough large (and if an area efficient tuning strategy is used). We mention that op amp tuning may be applied to all the circuits proposed in [9-15]; for all those circuits an auxiliary resistor (matched with the load resistor) is not required.

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