Low Voltage CMOS Current and Voltage References without Resistors

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***Abstract*—Here we describe low voltage current and voltage references which only use MOSFETs in strong inversion and pnp substrate transistors; both the references exhibit very good performance in terms of power supply rejection and do not require compensation capacitances; the minimum supply voltage is about 0.8V for the current reference and 1.2V for the voltage reference.**

I. INTRODUCTION

Bandgap voltage references [1-5] are very important building blocks in a variety of analog and mixed mode integrated systems. Although bandgap references have been widely used since their invention [4-5], the emergence of sub-micron CMOS processes has created new issues.

First, the reduction of the minimum feature size of MOS transistors also reduces the breakdown voltages, thus making it mandatory to reduce supply voltages. Beside this "reliability" constraint, other important reasons may exist for using low supply voltages (e.g. power consumption). As a result, several bandgap circuits working with supply voltages near, or even below, 1V have been reported in the last years [6-11].

Second, traditional bandgap circuits use resistors, which may be not available in many practical cases. In sub-micron CMOS processes the polysilicon layers and the source/drain regions are covered by a conductive material (e.g. titanium silicide) in order to reduce their sheet resistances [1]. Only in some cases a silicide block mask is available, so that relatively "high" sheet resistances are available; even in these cases, models for resistors are often not enough accurate [2].

The circuit shown in figure 1 allows to integrate a bandgap reference without using resistors [1]. However, this circuit is not suitable for low voltage operation; in [1] the supply voltage was 3.7V, which, clearly, is too high for most sub-micron systems. In this paper we describe CMOS voltage and current references which use only MOSFETs in strong inversion, do not need resistors and have a much lower minimum operating supply voltages. The paper is organized as follows: in section II the Buck current source is reviewed, while in section III a low voltage, self-biased current source without resistors is introduced and analyzed from a theoretical point of view; a simple model of the output current which allows an easy design of the current source is also proposed. In section IV low voltage current and voltage references designed in a standard 0.13 μm CMOS process are described and transistor level simulations are reported; conclusions are given in section V.

II. CURRENT SOURCE WITHOUT RESISTORS

In any bangap circuit, if the voltage reference must have a good power supply rejection, the currents used for biasing the "diodes" should be, as much as possible, independent on the supply voltage. This is not an issue in traditional bandgap circuits where self-biased PTAT/R current sources are already present in the bandgap circuit. However, if resistors may not be integrated, PTAT/R current sources are, clearly, not an option. This is an important issue for bandgap reference which do not use resistors, such as the reference in [1].

Fig. 1 shows the circuit proposed in [1]; the emitter area of Q_2 is n ($n > 1$) times bigger than the emitter area of Q_1 and the width of M_1 is m times ($m > 1$) bigger than the width of M_2, whereas their lengths are equal; M_3 and M_4 are (nominally) identical, so that

$$I_{E1} = I_{E2} = I_{SD1} = I_{SD2} = I_{OUT} \tag{1}$$

and the output current I_{OUT} may be mirrored by other PMOS transistors; the accuracy of the current mirrors is critical for correct operation (for instance, large transistors must be made by connecting in parallel many unit transistors [1]).

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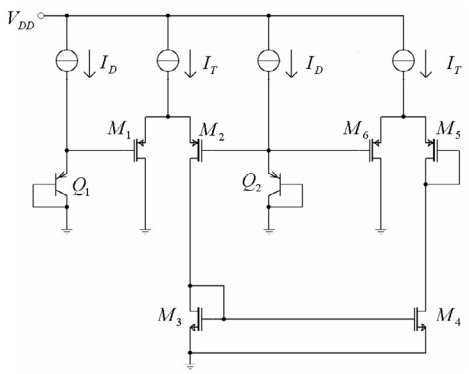

Figure 1. Bandgap reference which does not use resistors (see [1]).

If we neglect the base currents of Q_1 and Q_2 and mismatch

$$V_{EB1}+V_{SG1}=V_{EB2}+V_{SG2} \;\Rightarrow\; V_{EB1}-V_{EB2}=\frac{kT}{q}\ln(n)=V_{OV2}-V_{OV1} \qquad (2)$$

where k is the Boltzmann constant, T is the absolute temperature, q is the magnitude of the electron charge and the overdrive voltage V_{OV} is the difference between the gate to source voltage, V_{SG}, and the threshold voltage. Assuming that M_1 and M_2 are in strong inversion and neglecting channel length modulation

$$\begin{aligned} &I_{DS1}=\frac{1}{2}\mu_n c_{ox}\left(\frac{w_1}{L_1}\right)V_{OV1}^2=\frac{1}{2}\mu_n c_{ox}\left(\frac{w_2}{L_2}\right)V_{OV2}^2 \\ &\Downarrow \\ &\left(\frac{w_1}{L_1}\right)V_{OV1}^2=\left(\frac{mw_2}{L_2}\right)V_{OV1}^2=\left(\frac{w_2}{L_2}\right)\left[V_{OV1}+\frac{kT}{q}\ln(n)\right]^2 \end{aligned} \qquad (3)$$

Since $w_1=mw_2>w_2$, only one acceptable solution exists for the overdrive voltages, and therefore for the output current

$$\begin{aligned} &V_{OV1}=\left[\frac{kT}{q}\ln(n)\right]*\left(\frac{1+\sqrt{m}}{m-1}\right),\quad V_{OV2}=\left[\frac{kT}{q}\ln(n)\right]*\left(\frac{m+\sqrt{m}}{m-1}\right) \\ &I_{E1}=I_{E2}=I_{DS1}=I_{DS2}=I_{OUT}=\frac{1}{2}\mu_n c_{ox}\left(\frac{w_1}{L_1}\right)\left(\frac{1+\sqrt{m}}{m-1}\right)^2\left[\frac{kT}{q}\ln(n)\right]^2 \end{aligned} \qquad (4)$$

As evident from the last equation, the output current is independent on the supply voltage; this is, in fact, a "self-biased" circuit and start up circuitry (not shown in the figure) is necessary [12]. Since the bandgap voltage (i.e. about *1.2V*) is generated at the drain of M_4, this circuit requires a rather high supply voltage. Furthermore, if we consider channel length modulation, variations of the supply voltage produce significant variations of V_{SD2} and V_{DS3}, but small variations of V_{SD1} and V_{DS4}, resulting in errors of the current mirrors (M_1,M_2) and (M_3,M_4) which depend on the supply voltage; this ends up in a dependence of the output current on the supply voltage (i.e. low power supply rejection). In the next sections we describe an alternative solution which does not use resistors and has both a lower minimum operating supply voltage and a much higher power supply rejection.

III. Low voltage sub-micron CMOS current source without resistors

Let us consider the circuit in Fig. 2 (although the transistors M_4 and M_6 are connected in parallel, for the sake of clarity it is more convenient to draw them as different transistors). For correct operation of the current source I_0, V_{GS1} and V_{GS2} must be somewhat lower than, respectively, V_{EB1} and V_{EB2}. Since, in sub-micron CMOS systems, typical threshold voltages of NMOS transistors are in the order of *300mV*, the overdrive voltages (V_{OV1}, V_{OV2}) must be enough small (see later). The emitter area of Q_2 is n ($n > 1$) times bigger than the emitter area of Q_1 and the width of M_1 is m times ($m > 1$) smaller (in contrast with the previous circuit) than the width of M_2 whereas their lengths are equal; M_3, M_4, M_5 and M_6 are (nominally) identical. Furthermore, we assume (see later)

$$I_0=2I_{E1}=2I_{E2}=2I_{DS1}=2I_{DS2}=2I_{OUT} \qquad (5)$$

Under these assumptions,

$$V_{EB1}-V_{GS1}=V_{EB2}-V_{GS2} \;\Rightarrow\; V_{EB1}-V_{EB2}=\frac{kT}{q}\ln(n)=V_{OV1}-V_{OV2} \qquad (6)$$

so that

$$\left(\frac{w_1}{L_1}\right)\left[V_{OV2}+\frac{kT}{q}\ln(n)\right]^2=\left(\frac{w_2}{L_2}\right)V_{OV2}^2=\left(\frac{mw_1}{L_1}\right)V_{OV2}^2 \qquad (7)$$

Since $w_2=mw_1>w_1$, only one acceptable solution exists for the overdrive voltages

$$V_{OV1}=\left[\frac{kT}{q}\ln(n)\right]*\left(\frac{m+\sqrt{m}}{m-1}\right),\quad V_{OV2}=\left[\frac{kT}{q}\ln(n)\right]*\left(\frac{1+\sqrt{m}}{m-1}\right) \qquad (8)$$

With *m=4*, *n=10*, V_{OV1} and V_{OV2} are approximately *120mV* and *60mV* at room temperature (i.e. enough small). Comparing equations (4) and (8) it is evident that the nominal output currents of the circuits in Fig. 1 and in Fig.2 are similar. Again, in the circuit in Fig. 2, variations of the supply voltage produce significant variations of V_{DS1} and V_{SD4}, resulting in a dependence of the output current on the supply voltage. This issue is solved with the circuit shown in Fig. 3 (start up circuitry not shown): the differential amplifier allows proper operation of the current mirror (M_3,M_4) even at lower supply voltages and keeps V_{SD3} and V_{DS1} close to, respectively, V_{SD4} and V_{DS2}. The current source I_0 in Fig. 2 is implemented by M_{10}; the transistor M_8 is important for keeping V_{DS9} close to V_{DS10}. All PMOS transistors have almost "matched" source to drain voltages, thus providing a first order compensation of channel length modulation (the maximum difference between different V_{SD}

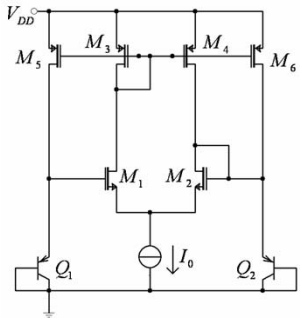

Figure 2. Proposed current reference.

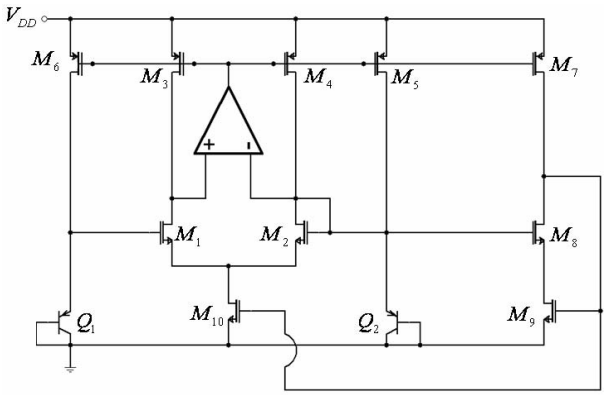

Figure 3. Proposed current reference with higher power supply rejection.

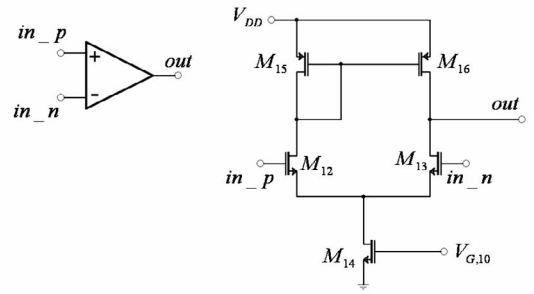

Figure 4. A simple implementation of the error amplifier shown in figure 3.

voltages is about $\left[kT\ln(n)/q\right]$, i.e. about *60mV* at room temperature if *n=10*); the reduction of current mirrors errors dependent on the supply voltage improves the power supply rejection of the current source. A simple implementation of the differential amplifier (see Fig. 3) is shown in Fig. 4; the transistors (M_{15},M_{16}) must have minimum channel length and be very wide (for keeping small the voltage across the "diode" M_{15}); the minimum operating supply voltage may be (only slightly) reduced if V_{DD} is included in the input common mode range of the differential amplifier (e.g. using a folded cascode [1]).

IV. Design and Simulations

A. Self-biased low voltage current source

The current reference shown in Fig. 3 and an associated voltage reference (see later) have been designed using the HCMOS9 0.13 μm CMOS process from ST Microelectronics. In the current reference, according to equations (3), (6), and (9), *n=8* and *m=4* so that the output current is about *10 μA* at *300K*. The bipolar transistors Q_1 and Q_2 have been implemented by means of lateral pnp devices (pnp substrate transistors could be a better choice from the point of view of the spread of the reference voltage [13], but those transistors are often not well characterized). All NMOS transistors have minimum channel length $(L_{\min})$; (M_3,M_4,M_5,M_6,M_7) have a channel length equal to $(4*L_{\min})$. Fig. 5 reports the output current of the circuit in Fig. 3 as a function of temperature; clearly, this current is not a PTAT current (while the ΔV_{GS} of M_1 and M_2 are PTAT voltages). Fig. 6 reports the output current as a function of the supply voltage.

B. Voltage reference

The voltage reference is obtained by connecting the gate of M_2 in Fig. 3 to one or more stages similar to the one implementing the ΔV_{GS} in Fig. 3 (M_1-M_4, M_{10} and the error amplifier); in our design we have used three stages. The reference voltage as a function of temperature and supply voltage is depicted in Fig. 7 and 8 respectively. Figure 9 shows the (positive) power supply gain of the voltage reference. These simulations confirm that, beside a lower minimum supply voltage, the proposed solution may offer a much better power supply rejection than the circuit in [1]; in fact, although in [1] very long channel transistors ($15\mu m$ in a $0.5\mu m$ CMOS process) have been used, the power supply rejection at *10Hz* was (*-45.1dB*) which is lower than in our design (*-52dB*, the maximum channel length is $(4*L_{\min})$ in a 0.13 μm CMOS process). A Monte Carlo simulation including the effect of mismatch has been run on both the current and voltage references using the statistical models provided by the foundry and the results are reported in Fig. 10. The low voltage start-up is a modified version of [12], in which the voltage divider has been implemented using MOS devices instead of resistors. The start-up transient response of the circuit is shown in Fig. 11.

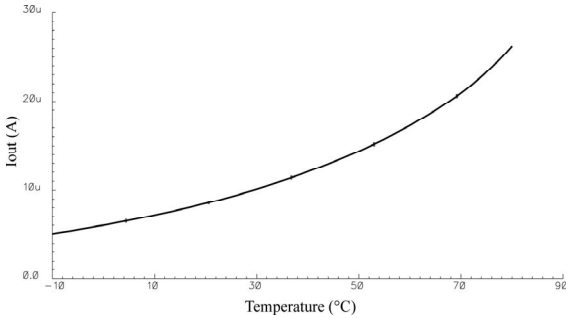

Figure 5. Output current as a function of the temperature.

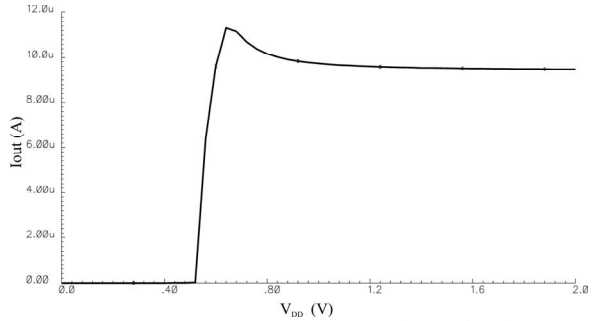

Figure 6. Output current as a function of the supply voltage.

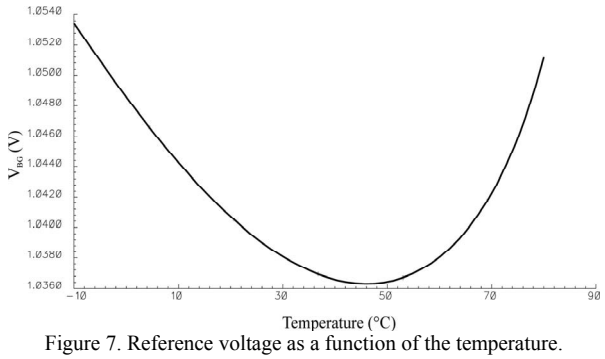

Figure 7. Reference voltage as a function of the temperature.

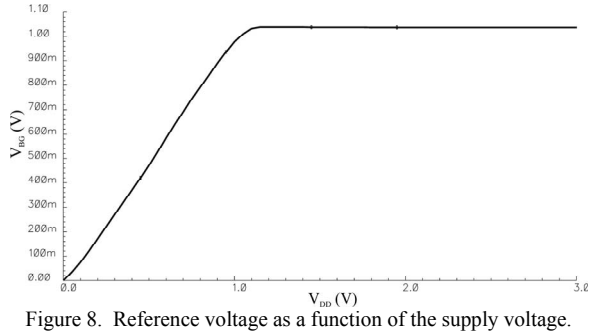

Figure 8. Reference voltage as a function of the supply voltage.

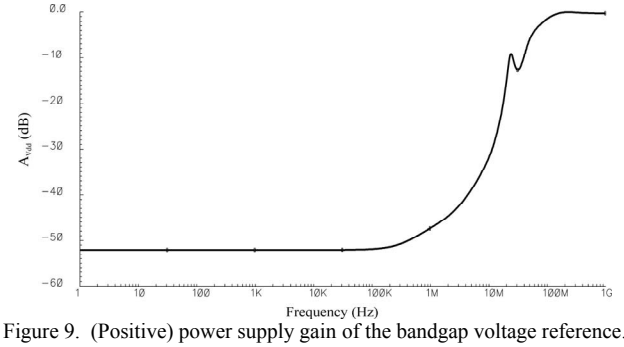

Figure 9. (Positive) power supply gain of the bandgap voltage reference.

V. CONCLUSIONS

We have described low voltage current and voltage references without resistors suitable to be implemented with sub-micron CMOS processes. Simulations in a standard 0.13 μm CMOS process have shown good temperature stability and excellent power supply rejection. Monte Carlo simulations including the effect of mismatches confirm the robustness of the circuit.

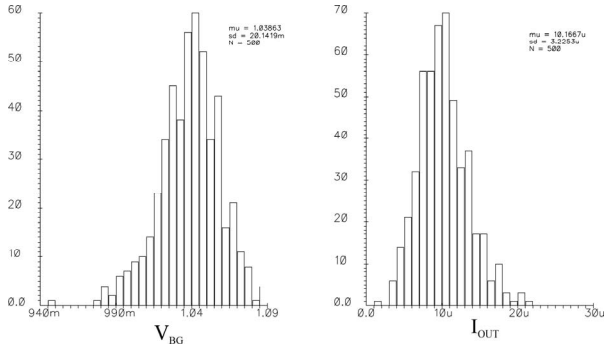

Figure 10. Monte Carlo simulation results.

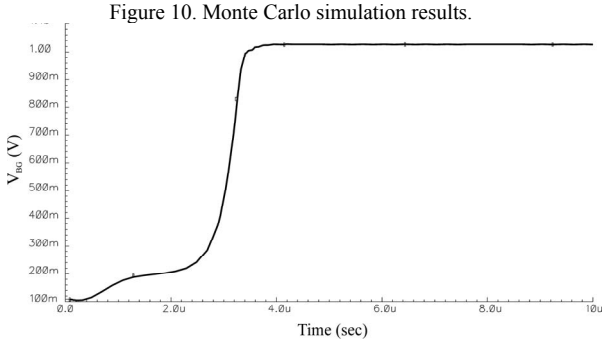

Figure11. Start-up transient of the reference voltage.

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