Low Voltage, Low Power, Compact, High Accuracy, High Precision PTAT Temperature Sensor for Deep Sub-micron CMOS systems

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Abstract— **Temperature measurement is becoming increasingly important in integrated circuits and microsystems; nevertheless, existing techniques for the integration of high accuracy, high precision temperature sensors are not optimal for deep sub-micron CMOS processes. Here we describe a low voltage, low power, compact, high accuracy, high precision temperature sensor for deep sub-micron CMOS systems; our approach takes advantage of charge balancing and charge sharing for low current consumption, does not use resistors for compactness, and takes advantage of both PTAT and autozero techniques for high accuracy and high precision; the circuit can be operated at low supply voltages. As a proof of concept, we report transistor level simulations in a standard 0.13µm process; the sensor only sinks about $6\mu A$ from a $1.2V$ supply voltage, achieving a power dissipation as low as $7.2\mu W$.**

I. INTRODUCTION

Temperature measurement is very important in integrated circuits and microsystems; in fact, physical, chemical, and biological properties generally depend on temperature, so that estimating the temperature is essential in many applications, including pressure sensors, µTAS, Lab-on-Chip, BioMEMS and chemical sensors. In many cases the limits on the supply voltage and power consumption are not too severe; as an example, if the temperature of a microsystem [1-4] must be controlled, heating or cooling typically require more power than just measuring the temperature. Moreover, there are ultimate limits; for instance, one of the problems with low currents is the obvious requirement that the important currents in the circuit should be enough larger than leakage currents (a problem which becomes more important at high temperature). However, in many applications it would still be very important to measure the temperature (with reasonable accuracy and precision) with a very low power consumption, using a low supply voltage, and occupying a small silicon area. This could, for instance, be the case of a wireless temperature sensor powered by the energy harvested from the environment. As another example, in high performance digital VLSI circuits, the reduction of the minimum feature size of CMOS transistors typically results in an increased power consumption per unit area; however, since excessive temperature is one of the most important failure mechanisms for integrated circuits, it would be important to monitor the chip temperature; in some cases it could even be useful to monitor the temperature in various positions of the chip (in this case, many low power, low voltage, compact temperature sensors should be integrated on chip). Clearly, since calibration unavoidably introduces additional costs, the accuracy [5] and precision [5] of the temperature sensors should, possibly, be acceptable without calibration or, at least, after a simple calibration procedure; this problem would be even more critical for an array of compact temperature sensors on the same silicon chip, as the separate calibration of each temperature sensor would, clearly, be complex and expensive.

Many integrated temperature sensors have already been reported (e.g. [6-12]); even in CMOS processes [8-12] the best device for temperature sensing is the bipolar junction transistor [13] and, in particular, the *pnp* substrate transistor [14-16]. However, existing techniques for integrating CMOS temperature sensors are not optimal for deep sub-micron processes: first, the minimum supply voltage is typically above $2.5V$; second, resistors are included (in deep sub-micron CMOS processes, the sheet resistance of both polysilicon layers and source/drain regions is deliberately reduced by a conductive coating; even if a silicide block mask is available, resistors are often not enough accurate and, last but not least, occupy a large chip area, especially if low power consumption is an issue); third, the need of high accuracy, high precision op amps increases the overall current consumption.

Here we describe a low voltage, low power, compact, high accuracy, high precision temperature sensor which is suitable for integration in deep sub-micron CMOS systems. In fact, first, a low supply voltage is possible (in our design example we have used $1.2V$); second, resistors are not necessary; third, we use charge balancing and charge sharing for low current

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consumption; PTAT techniques and an autozero comparator might allow to achieve a satisfactory accuracy and precision even in absence of calibration, which would be an important feature for an "array" of compact temperature sensors integrated on the same VLSI chip. Clearly, our strategy could also be advantageous for wireless, low voltage, low power, battery powered temperature sensors. As a proof of concept, we describe a low voltage, low power, compact temperature sensor designed in a standard 0.13µm CMOS process.

II. Charge Balancing, Charge Sharing, Low Power PTAT Temperature Sensor

The proposed temperature sensor (see Fig. 1) takes advantage of charge balancing for temperature sensing (this general approach is discussed in detail in [10]). In our system, the voltages v_{BE} and Δv_{BE} (with $\Delta v_{BE}<0$) are preliminarily stored across, respectively, the capacitors C_{vBE} and C_{PTAT} (pre-charge phase, *pre*); then either C_{vBE} or C_{PTAT} is connected in parallel to C_X (charge-sharing phase, *CS*), depending on the sign of v_X (the signals *pre* and *CS are standard non-overlapping phases clocks*). In practice, the positive voltage v_{BE} and the negative voltage Δv_{BE} alternatively charge C_X and the feedback loop keeps the average charge accumulated on C_X close to zero (the loop is closed by the control signals c_1 and c_2). Fig. 2 shows the typical time evolution of v_X, *c1* and *clk*; *CS* is simply a delayed version of *CS* and enables the edge triggered D-type flip-flop. The negative PTAT voltage Δv_{BE} can be obtained by taking the difference between the emitter to base voltages of two identical *pnp* substrate transistors running at different collector currents (see later); it is therefore evident that the generation of both v_{BE} and Δv_{BE} does not, in principle, require resistors or op amps. Furthermore, the proposed structure takes advantage of charge sharing for increasing or reducing (depending on the sign of v_X) the charge accumulated on C_X; in fact, if two capacitors C_1 and C_2, having initial voltages equal, respectively, to v_1 and v_2, are connected in parallel, the final voltage v_f across the two capacitors will be

$$v_f = \frac{C_1 v_1 + C_2 v_2}{C_1 + C_2}. \tag{1}$$

Obviously, the charge sharing approach does not require resistors or op amps; furthermore, low capacitances (i.e. small area) will give low currents, potentially resulting in compact, low power temperature sensors (in other words, we use a compact, switched capacitor equivalent of a large resistor).

The temperature can be derived by counting the number of clock cycles N_{PTAT} (bitstream c_1 is one) and N_{vBE} (bitstream c_1 is zero) in a total number of clock cycles N_{TOT}.

The voltage v_X can be obtained by iterating (1), as follows:

$$v_X|_i = \begin{cases} \dfrac{C_X v_X|_{i-1} + C_{PTAT}\Delta v_{BE}}{C_X + C_{PTAT}}, & v_X|_{i-1} > 0 \\ \dfrac{C_X v_X|_{i-1} + C_{v_{BE}} v_{BE}}{C_X + C_{v_{BE}}}, & v_X|_{i-1} < 0 \end{cases} \tag{2}$$

where *i* is the index for the clock cycles.

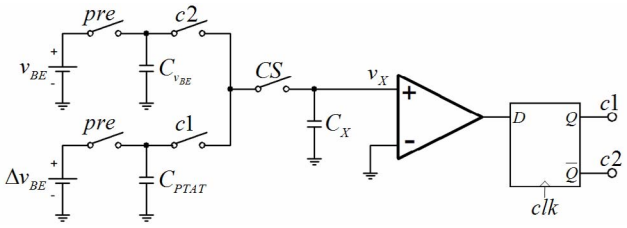

Figure 1. Temperature sensor using charge balancing and charge sharing

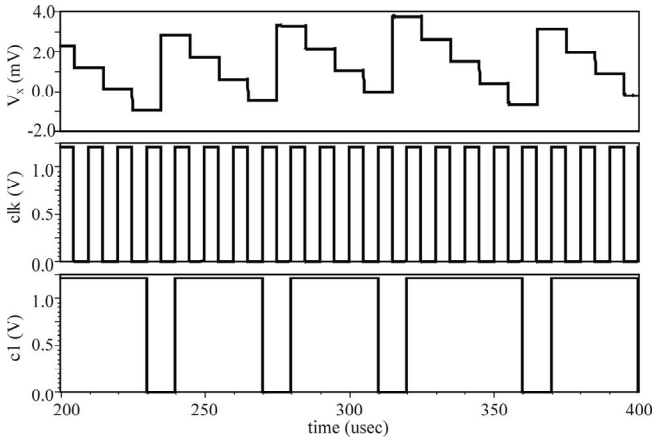

Figure 2. Voltage v_X and clok signals as a function of time.

If $C_X >> C_{PTAT}$ and $C_X >> C_{vBE}$ we may obtain the variations of the charge accumulated on C_X in both cases:

$$\Delta Q_{X,i} = C_X\left[v_X|_i - v_X|_{i-1}\right] \simeq \simeq \begin{cases} \dfrac{C_X C_{PTAT}}{C_X + C_{PTAT}}\Delta v_{BE}, & v_X|_{i-1} > 0 \\ \dfrac{C_X C_{v_{BE}}}{C_X + C_{v_{BE}}} v_{BE}, & v_X|_{i-1} < 0 \end{cases} \tag{3}$$

Taking into account the feedback loop (i.e. charge balancing), if we consider a sufficiently long time interval, we find

$$N_{PTAT}\frac{C_X C_{PTAT}}{C_X + C_{PTAT}}\Delta v_{BE} + N_{vBE}\frac{C_X C_{v_{BE}}}{C_X + C_{v_{BE}}} v_{BE} = 0 \tag{4}$$

Since $C_X >> C_{PTAT}$ and $C_X >> C_{vBE}$ the previous expression can be simplified as follows

$$N_{PTAT} C_{PTAT}\Delta v_{BE} + \left(N_{TOT} - N_{PTAT}\right) C_{v_{BE}} v_{BE} = 0 \tag{5}$$

so that ($\Delta v_{BE}<0$))

$$N_{PTAT} = \frac{N_{TOT} C_{v_{BE}} v_{BE}}{C_{v_{BE}} v_{BE} - C_{PTAT}\Delta v_{BE}} = \frac{N_{TOT} C_{v_{BE}} v_{BE}}{C_{v_{BE}} v_{BE} + C_{PTAT}\left|\Delta v_{BE}\right|}. \tag{6}$$

III. Low Voltage, Low Power, Compact PTAT Temperature Sensor for Deep Sub-micron CMOS Systems: Design and Simulations

The complete sensor has been designed in a standard $0.13\mu m$ CMOS process from ST Microelectronics; the supply voltage, the clock frequency, and the conversion time were, respectively, $1.2V$, $f_{CS}=100KHz$, and $10ms$. The capacitance values were

$$C_X = 100\,pF, C_{PTAT} = 2\,pF, C_{vBE} = 0.5\,pF\,. \qquad (7)$$

The negative PTAT voltage Δv_{BE} can be obtained by taking the difference between the emitter to base voltages of, respectively, Q_1 and Q_2, which are two nominally identical *pnp* substrate transistors running at different collector currents (the collector current of Q_2 is larger so that the PTAT voltage is negative). Figure 4 shows both the low voltage circuit and the nominal values of the biasing currents at room temperature; the currents ($I_1=100nA$ and $I_2=1\mu A$) allow a satisfactory precharge of the capacitances C_{PTAT} and C_{vBE}; furthermore, the important currents must be larger than the correspondent parasitic currents (e.g. leakage). In order to generate sub-μA currents in a small silicon area, for our preliminary tests we have used the very simple strategy described, for instance, in [17] (long-channel PMOS devices are operated in deep triode region in order to mimic a large resistor; see M_3 and M_4 in Fig. 3); however, slightly more sophisticated circuit topologies could be used for reducing the spread of these currents (e.g. see [18-20]).

A low power (non-autozeroed) comparator is shown in Fig. 4. However, beside the correction of the input offset and 1/f noise voltages [5,8,21], the comparator should also have a very high open-loop gain so that its output saturates to 0 or V_{DD} even when v_X is very small in such a way that the sign of v_X can be accurately detected (a low gain of the comparator would easily limit the resolution [5] of the entire sensor); the high gain is achieved by cascading two comparators and by applying to the first comparator an autozero strategy with gain enhancement [21], using a $10pF$ capacitor; each comparator, as shown in Fig. 4 has two gain stages and the long channel transistors (M_3 and M_4). The switches shown in Fig. 1 are implemented by using MOSFETs with a thicker oxide, thus reducing their leakage currents, which are critical at high temperature and with low clock frequencies.

The typical time evolution of v_X has already been shown in Fig. 2 (which was obtained with the complete CMOS sensor). Although high clock frequencies reduce leakage, they also tend to require larger currents (e.g. precharging the capacitors C_{PTAT} and C_{vBE} in a smaller time interval would require higher biasing currents for Q_1 and Q_2). Fig. 5 shows N_{PTAT} as a function of temperature in different cases: the continuous line represents the ideal case obtained from the analytic model discussed above; the dashed line represents the CMOS system when ideal voltage sources are used to charge both C_{PTAT} and C_{vBE}; the dotted line is the simulation of the complete CMOS temperature sensor; the resolution is about $1°C$ in the temperature range ($0°C$ – $60°C$). The complete temperature sensor only sinks about $6\mu A$ from a $1.2V$ supply voltage, resulting in a power dissipation equal to about $7.2\mu W$.

Since the total power consumption is dominated by the comparator, it would seem that further reductions of the power consumption are possible; however, since previously reported CMOS PTAT temperature sensors generally use about 30-300μA from supply voltages which are typically above $2.5V$, our simulations already demonstrate the potentialities of the proposed approach.

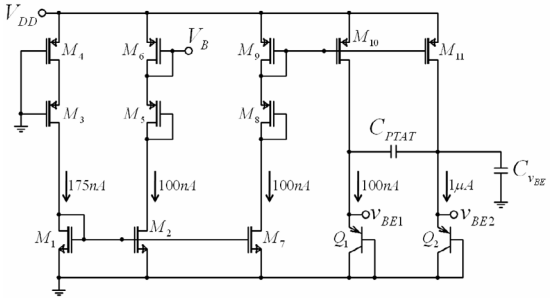

Figure 3. Biasing circuitry.

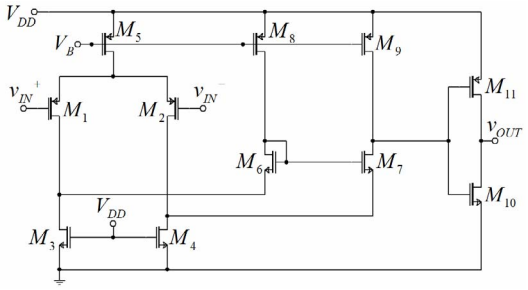

Figure 4. Comparator.

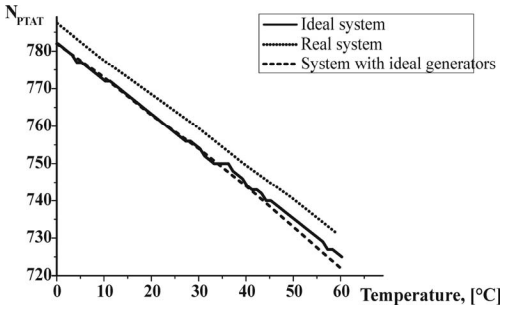

Figure 5. N_{PTAT} as a function of temperature.

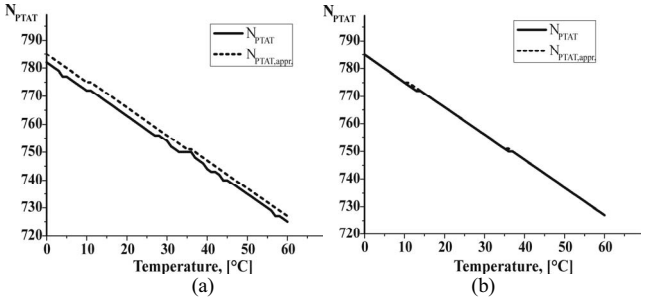

Figure 6. Comparison of simulations against the approximated model

Figures 6a and 6b report the comparison of the transistor level simulations against the approximated model given in (6) and the ideal model which can be found by using the exact, recursive relation given in (2) in the following two cases:

$$\begin{aligned} a &\rightarrow C_X = 100\,pF, C_{PTAT} = 2\,pF, C_{vBE} = 0.5\,pF, \\ b &\rightarrow C_X = 100\,pF, C_{PTAT} = 0.2\,pF, C_{vBE} = 0.05\,pF \end{aligned} \quad (8)$$

Clearly, in the case b the model (6) is more accurate (the conditions for determining the approximate model (6) are $C_X >> C_{PTAT}$ and $C_X >> C_{vBE}$).

Finally, the area of the proposed circuit is likely to be dominated by C_X; in our simulations C_X has been implemented as a Poly/Nwell thick oxide capacitor; with this choice, the estimated area (about 0.015 mm^2) is much lower than the area of previously reported CMOS PTAT temperature sensors which typically occupy more than $2mm^2$.

CONCLUSIONS

In this paper we have proposed a charge balancing, charge sharing, low voltage, low power, compact, high accuracy, high precision CMOS PTAT temperature sensor which can be integrated in deep sub-micron CMOS systems. In fact, first, a low supply voltage is possible (in our design example we have used $1.2V$); second, resistors are not necessary; third, we use both charge balancing and charge sharing for low power consumption. PTAT techniques and an autozero comparator can result in both acceptable accuracy and precision even in absence of calibration, which would be an important feature for an "array" of compact temperature sensors integrated on a single VLSI chip. Clearly, our strategy could be advantageous for many other applications, such as temperature sensors powered by batteries or by energy somehow harvested from the environment. As a proof of concept, we have designed a temperature sensor in a standard 0.13µm process; although the comparator dissipates the largest portion of the total power, the complete sensor only sinks about $6\mu A$ from a $1.2V$ supply voltage, resulting in a power dissipation equal to about $7.2\mu W$, which is about 10-100 times smaller than previously reported solutions; the resolution was about $1°C$ in the temperature range ($0°C - 60°C$) for a conversion time of just $10ms$.

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