Analog Integr Circ Sig Process (2009) 58:81–90
DOI 10.1007/s10470-008-9234-1

On-chip low drop-out voltage regulator with NMOS power transistor and dynamic biasing technique

Gianluca Giustolisi · Christian Falconi · Arnaldo D'Amico · Gaetano Palumbo

Received: 8 February 2007 / Revised: 5 September 2007 / Accepted: 9 October 2008 / Published online: 26 November 2008

Abstract We propose a NMOS low drop-out voltage regulator suitable for on-chip power management. The circuit does not requires any external components for achieving compensation since it is internally compensated. A dynamic biasing strategy and a clock booster allows to properly drive the NMOS power transistor in a power efficient fashion and without limiting the speed response of the regulator. Transistor level simulations confirm the effectiveness of the proposed approach.

Keywords CMOS analog integrated circuits · Voltage reference · CMOS reference · Low-drop voltage regulator

G. Giustolisi (✉) · G. Palumbo
Department of Electric, Electronic and System Engineering, University of Catania, Catania, Italy
e-mail: ggiustolisi@diees.unict.it

G. Palumbo
e-mail: gpalumbo@diees.unict.it

C. Falconi · A. D'Amico
Department of Electronic Engineering, University of Tor Vergata, Rome, Italy
e-mail: falconi@eln.uniroma2.it

A. D'Amico
e-mail: damico@eln.uniroma2.it

C. Falconi · A. D'Amico
CNR Institute of Acoustics "O. M. Corbino", Via Fosso del Cavaliere 100, 00133 Rome, Italy

1 Introduction

In recent years, power management in integrated circuits (ICs) is gaining more and more attention since it allows to drastically reduce the standby power of portable equipments such as cellular phones and PDAs [1]. In the case of a mixed-signal IC, a typical scenario may be composed of high voltage blocks (i.e., I/O buffers powered at 1.8 V for compatibility reason), of medium voltage blocks (i.e., analog circuits such as PLLs or operational amplifiers powered at 1.2–1.4 V) and of low voltage blocks (i.e., the logic circuit working at 0.6–1 V). Whereas, in the case of a digital IC, we may have speed-critical logic circuits working at nominal voltage (i.e., 1.2 V) and noncritical circuits powered at a lower supply (i.e., 0.9 V) thus reducing power dissipation [2].

A typical on-chip power management architecture consists of a single power supply (e.g., and external battery) and one or more local Voltage Regulators (VR) used to power up different sub-blocks at different supply voltages [3]. Such a strategy not only does allow for supplying different blocks at different voltages but also can significantly reduce crosstalk, improve the voltage regulation, eliminate spikes due to bondwires and reduce both board space and external pins [1].

Voltage regulators are made up of a stable and temperature independent voltage reference (V_{REF}), an error amplifier and a large power transistor designed to deliver the current to the load, Z_L. In MOS technology, depending on whether the output transistor is an N- or P-type we may have the two general architectures shown in Fig. 1. The NMOS topology in Fig. 1(a) is the natural and the first choice for implementing a voltage regulator since it has many advantages (low output resistance, straightforward compensation, better load regulation, lower area

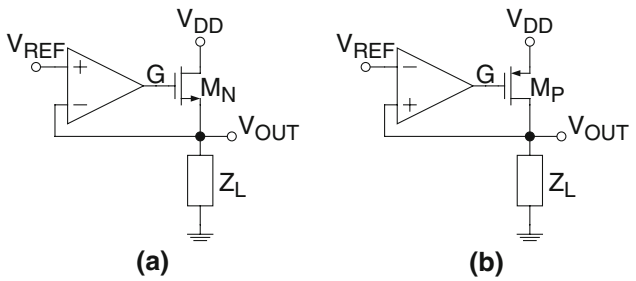

Fig. 1 Main schema of voltage regulators. **a** NMOS voltage regulator. **b** PMOS voltage regulator

occupation, etc.). However, it is not suitable for low-voltage applications. In fact, since node G cannot go above the supply voltage, V_{DD}, the output voltage, V_{OUT}, is limited to $V_{DD} - V_{GS}$ where V_{GS} depends on the load current, I_L [4].

Today, in several CMOS systems the supply voltage is so low that PMOS LDO (Low Drop-Out) Voltage Regulators are preferable and the topology in Fig. 1(b) is often adopted [3, 5–9]. However, PMOS LDO regulators have several problems. In fact, the output pole (i.e., associated to the output node of the voltage regulator) is both unpredictable and located at a rather low frequency, making the frequency compensation complex. Therefore, PMOS LDO regulators, in general, need a large external capacitor for closed loop stability; additionally, little tolerance is allowed on both the capacitance and the parasitic series resistance of the external capacitor since both are used to achieve compensation. Besides, load regulation is degraded and the maximum output current (for a given area occupied by the output transistor) is significantly lower due to the reduced current capability of PMOS transistors [2, 10–12].

To solve the compensation difficulties and the necessity of a large external capacitor, NMOS low drop-out regulators have been reintroduced. In fact, these circuits may be compensated internally provided that the output capacitor is maintained below a certain value as is the case of on-chip voltage regulators.

In order to perform low-dropout operation, two different approaches have been used to make the NMOS gate rise over the supply voltage. In the first one the error amplifier is powered by a supply higher than V_{DD}. Charge pumps [13–15] or a contactless inductive supply [16] have been used to do the job. However charge pumps have poor load efficiency and requires large capacitors resulting in high power and area consumption. Correspondingly, the contactless inductive supply is application specific and cannot be implemented anywhere. Moreover, in both cases, the fact that some current is not sinked from V_{DD} but from 2 V_{DD} (or more) results in a significantly larger "effective" quiescent current and power dissipation.

The second approach exploits floating gate devices to implement a voltage shifter connected between the output of the error amplifier and the gate of the NMOS transistor [4, 17]. However, not only do floating gate devices require specific technologies but also must be set up and programmed, resulting in an increased complexity of the regulator.

In this paper we propose a new NMOS LDO Voltage Regulator suitable for on-chip voltage regulation which makes use of a dynamic biasing strategy to properly drive the gate of the power transistor.

2 Basic principle

The basic principle of the proposed NMOS LDO Voltage Regulator is shown in Fig. 2 where a proper voltage shifter (represented by a battery of voltage V_B) allows to boost up the node G over V_{DD}, when necessary.

Obviously, the value of V_B must be chosen carefully. Assuming the output node of the operational amplifier (i.e., node H) can swing from V_{DS}^{sat} to $V_{DD} - V_{DS}^{\mathrm{sat}}$, node G can swing from $V_G^{\min}$ to $V_G^{\max}$, where

$$V_G^{\min} = V_B + V_{DS}^{\mathrm{sat}} \tag{1a}$$

$$V_G^{\max} = V_B + V_{DD} - V_{DS}^{\mathrm{sat}} \tag{1b}$$

Noting that $V_G = V_G^{\min}$, the circuit must be able to switch off the output transistor (i.e., with a large load, the transistor must be close to interdiction), it is necessary to satisfy the condition

$$V_{GS}^{\min} = V_G^{\min} - V_{\mathrm{OUT}} \leq V_{THN} \tag{2}$$

being V_{THN} the threshold voltage of M_N. Therefore, the voltage V_B should be as high as possible, provided that

$$V_B \leq V_{\mathrm{OUT}} + V_{THN} - V_{DS}^{\mathrm{sat}} \tag{3}$$

Clearly, if the supply voltage, V_{DD}, is lower than $V_{\mathrm{OUT}} + V_{THN} - V_{DS}^{\mathrm{sat}}$, the highest possible value for V_B is V_{DD} itself, so that the optimal value for V_B is

$$V_B = \min\left(V_{\mathrm{OUT}} + V_{THN} - V_{DS}^{\mathrm{sat}}, V_{DD}\right) \tag{4}$$

When the circuit is required to provide the maximum current to the load and the supply voltage is close to the

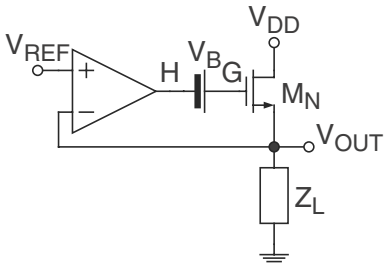

Fig. 2 Basic principle of the proposed LDO voltage regulator

output voltage of the regulator (worst case), the transistor M_N is almost certainly in the triode region and the load current can be modeled by

$$I_D = \mu_n C_{\rm ox}\left(\frac{W}{L}\right)_N\left(V_{GS} - V_{THN} - \frac{V_{DS}}{2}\right)V_{DS} \tag{5}$$

For a given minimum drop-out, $V_{\rm DO} = V_{DD}^{\rm min} - V_{\rm OUT}$, and a given maximum load current, $I_L^{\rm max}$, (corresponding to $V_{GS}^{\rm max} = V_G^{\rm max} - V_{\rm OUT} = V_B + V_{DD} - V_{DS\rm sat} - V_{\rm OUT}$), the aspect ratio of the MOS output transistor, $(W/L)_N$, should be

$$\left(\frac{W}{L}\right)_N = \frac{I_L^{\rm max}}{\mu_n C_{\rm ox}\left(V_B + V_{DD} - V_{DS\rm sat} - V_{\rm OUT} - V_{THN} - \frac{V_{\rm DO}}{2}\right)V_{\rm DO}} \tag{6}$$

Depending on the value of V_B see (3), (6) may be simplified into

$$\left(\frac{W}{L}\right)_N \approx \begin{cases} \frac{I_L^{\rm max}}{\mu_n C_{\rm ox} V_{DD} V_{\rm DO}} & \text{for } V_{DD} > V_{\rm OUT} + V_{THN} - V_{DS}^{\rm sat} \\ \frac{I_L^{\rm max}}{\mu_n C_{\rm ox}(V_{DD} - V_{THN}) V_{\rm DO}} & \text{for } V_{DD} < V_{\rm OUT} + V_{THN} - V_{DS}^{\rm sat} \end{cases} \tag{7}$$

where we considered $V_{DD} \gg 2\,V_{DS}^{\rm sat} + V_{\rm DO}/2$.

It is worth noting that the model in (7) underestimates the required aspect ratio since it does not take into account parasitic resistances, which must be considered for large load currents.

The regulator may be generalized by interposing a resistive voltage divider between the output of the regulator and the inverting input terminal of the error amplifier. In this case, it is easy to extend the present results by considering the general expression $V_{\rm OUT} = \beta V_{\rm REF}$, being β the feedback factor imposed by the resistive voltage divider.

3 Dinamically biased NMOS LDO regulator

The proposed NMOS LDO Regulator makes use of the dynamic biasing technique for implementing the voltage shifter, V_B [18], as shown in Fig. 3. Capacitor C_S acts as the voltage shifter and is charged to V_B by the Switched-Capacitor (SC) network in the figure.

The SC network requires two disoverlapped phases ϕ_1 and ϕ_2 of period T_S and works as follows. During phase ϕ_1 switches S_1 and S_2 are closed and the flying capacitor C_R is charged at V_B. Conversely, during phase ϕ_2, S_3 and S_4 close, C_R is connected in parallel to C_S and the charge is redistributed between the two capacitors.

In the z-domain, we have that, during the phase ϕ_1, the charges across both capacitors are [19]

$$Q_{CR}\left(z^{-\frac{1}{2}}\right) = C_R V_B\left(z^{-\frac{1}{2}}\right) = C_R V_B \tag{8a}$$

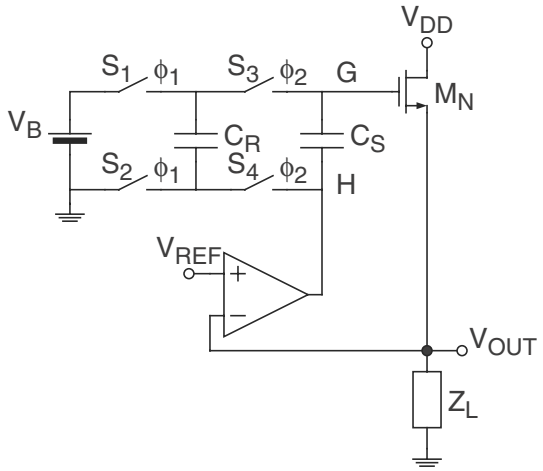

Fig. 3 Real implementation of the proposed NMOS LDO voltage regulator

$$Q_{CF}\left(z^{-\frac{1}{2}}\right) = C_S V_{GH}\left(z^{-\frac{1}{2}}\right) = C_S V_{GH}\left(z^{-1}\right) = C_S V_{GH}(z) z^{-1} \tag{8b}$$

where we considered the fact that V_B is a constant voltage and that the value of V_{GH} does not change during the phase ϕ_1. Moreover, during the phase ϕ_2, the charges become

$$Q_{CR}(z) = C_R V_{GH}(z) \tag{9a}$$

$$Q_{CF}(z) = C_S V_{GH}(z) \tag{9b}$$

Since during the phase ϕ_2 the charge is only redistributed between the two capacitors, we may write

$$Q_{CR}\left(z^{-\frac{1}{2}}\right) + Q_{CF}\left(z^{-\frac{1}{2}}\right) = Q_{CR}(z) + Q_{CF}(z) \tag{10}$$

that, considering (8) and (9) leads to

$$V_{GH}(z) = \frac{\frac{C_R}{C_R + C_S}}{1 - \frac{C_S}{C_R + C_S} z^{-1}} V_B \tag{11}$$

Relationship (11) represent the transfer function of a Switched-Capacitor (SC) integrator [19] that, after reaching the steady-state, will store the voltage V_B across the shifting capacitor C_S. The switches and the capacitor C_R perform an equivalent resistor $R_{\rm eq} = T_S/C_R$. The time constant of the integrator is $\tau_i = R_{\rm eq} C_S = T_S C_S / C_R$ and the settling time, t_s, after which we may consider C_S completely charged at V_B results

$$t_s = 4 T_S \frac{C_S}{C_R}. \tag{12}$$

3.1 Switches and phases generator

A particular attention is required in the design of the switches as well as of their driving signals. In fact, due to the large swing at nodes H and G some switches could not switch on properly. In our implementation we used a clock booster approach for driving the switches.

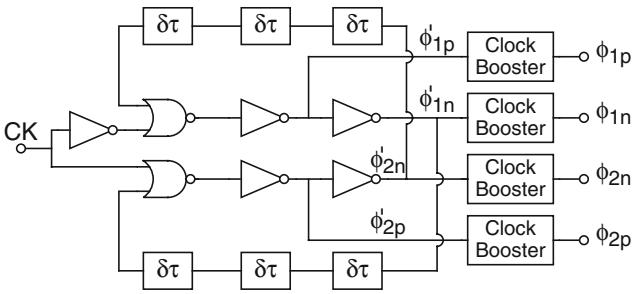

Fig. 4 4-Phase clock generator ($\delta\tau$ = delay blocks)

Switches S_1, S_2 and S_4 are implemented with minimum-sized NMOS transistors while S_3, which must handle the highest voltage in the circuit, is realized with a minimum-sized transmission gate (a minimum sized NMOS transistor in parallel with a PMOS one). Bulks of NMOS transistors are connected to ground while the bulk of the PMOS transistor of S_3 is connected to node G which is always at the higher potential.

Switches driving signals are generated by the circuit in Fig. 4. Starting from a master clock, CK, the circuit produces two main disoverlapped phases, ϕ'_{1n} and ϕ'_{2n}, and their respective complementary signals, ϕ'_{1p} and ϕ'_{2p}. These signals swing from ground to V_{DD} and are then passed to a Clock Booster block for being boosted up well above the supply voltage.

Clock boosters shown in Fig. 4 are implemented as shown in Fig. 5 [20]. Each of them consists of diode D_0, two capacitors, C_1 and C_2, and the NMOS transistor, M_0. Assuming an n-well CMOS process, the diode is implemented with the PN junction placed between the p^+ drain/source diffusions and the well. Capacitor C_{par} accounts for the parasitic capacitor given by the overall gate capacitance associated with the switches in the SC circuit.

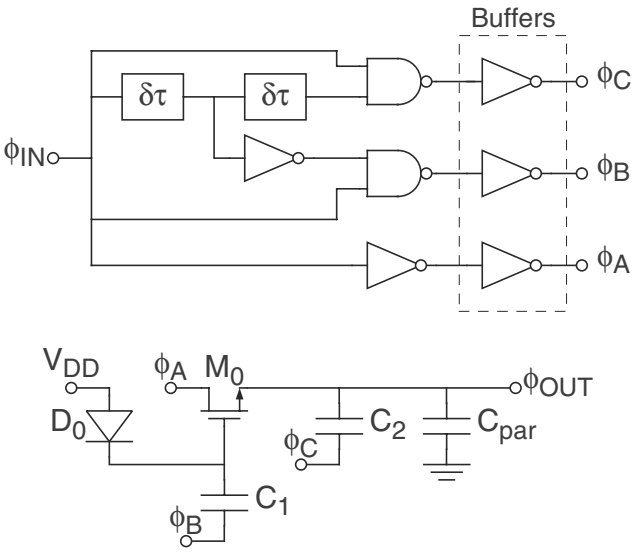

Fig. 5 Clock booster schematic

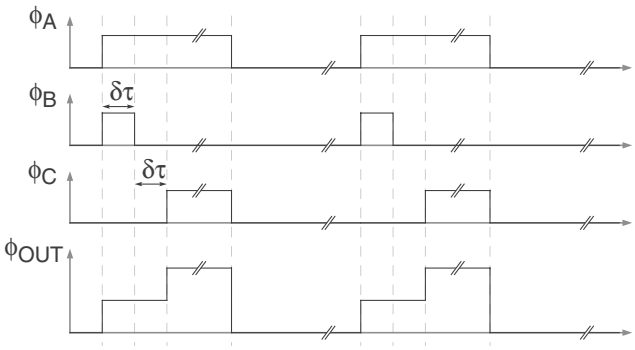

Fig. 6 Clock booster timing diagram

The digital section takes the phase ϕ_{IN} and produces the control signals ϕ_A, ϕ_B and ϕ_C, depicted in the timing diagram in Fig. 6 where, for clarity's sake, the time axis has been expanded. Specifically, when input ϕ_{IN} is high, it is quickly transferred to both phases ϕ_A and ϕ_B. After a delay of $\delta\tau$, ϕ_B goes down and remains in this condition until the next rising edge of the input occurs. After a second delay of $\delta\tau$, ϕ_C also goes high, and together with phase ϕ_A, remains in this condition until the next falling edge of the input takes place. To achieve both signal inversion and proper load driving, buffers may be included.

Referring to Fig. 5, after the start-up transient, diode D_0 will keep capacitor C_1 precharged to a voltage close to V_{DD}. During phases ϕ_A and ϕ_B with phase ϕ_C off, transistor M_0 is switched on (its gate is at 2 V_{DD}) and capacitor C_2 is precharged to V_{DD}. After charging C_2, phase ϕ_B goes down turning M_0 off, ϕ_C then goes up, and the output is boosted above the power supply by about V_{DD}. More precisely, there is a charge redistribution between capacitors C_2 and the parasitic capacitor, C_{par}, which sets ϕ_{OUT} to

$$\phi_{OUT}^{high} = \left(1 + \frac{C_2}{C_2 + C_{par}}\right) V_{DD} \tag{13}$$

Finally, when phases ϕ_A and ϕ_C go down, transistor M_0 is driven from the cut-off to the triode region, C_2 and C_{par} discharge through M_0, and the output goes to zero. The behavior of ϕ_{OUT} is shown in Fig. 6, too.

3.2 Switching noise

The dynamic biasing circuitry seems to add undesired noise to the output voltage of the regulator. Actually, due to the feedback, this effect is strongly mitigated.

It is apparent that noise may be introduced to node G of Fig. 3 either through charge injection or through leakage effects.[1] In both cases the noise can be modeled by means of a variation of the potential at node G, ΔV_G. If the noise

[1] Node H is dynamically at ground and no noise can be injected to this node.

makes node G to increase, due to the common drain configuration of M_N, voltage V_{OUT} increases, too. Therefore, due to the negative feedback, node H decreases and, since V_G follows V_H, node G is brought to the correct potential thus nullifying the effect of the noise. The time for this to happen is strictly related to the transition frequency of the loop gain, $\omega_T = 1/\tau_c$. Specifically, noises "slower" than τ_c are well compensated and mitigated by the feedback while noises "faster" than τ_c are not.

As a consequence, choosing a sampling period, T_S, smaller than τ_c always guarantees that both charge injection and leakage effects are nullified by the feedback loop.

4 Circuit design and simulations

The proposed NMOS LDO regulator was designed in a standard 0.35-μm CMOS process whose main parameters are $V_{THN0} = 0.55$ V, $V_{THP0} = -0.6$ V, $\mu_n C_{\mathrm{ox}} = 175\,\mu\mathrm{A/V}^2$ and $\mu_p C_{\mathrm{ox}} = 60\,\mu\mathrm{A/V}^2$. The reference voltage $V_{\mathrm{REF}} = V_{\mathrm{OUT}}$ was set to 1 V.

Considering $V_{THN} \approx 0.6$–0.7 V (the threshold voltage is greater than V_{THN0} due to the body effect) and $V_{DS}^{\mathrm{sat}} \approx 0.1$–$0.2$ V, the relationship (3) suggests a shifting voltage of 1.4 V. The shifting voltage is generated by the circuit in Fig. 7 where transistor aspect ratios and current I_B are designed to provide $V_B = 1.4$ V. Note that, if $V_{DD} < 1.4$ V, M_2 enters the triode region and the circuit generates $V_B \approx V_{DD}$ which is the best value allowed in this condition (see 4).

From (7) we set the width and length of the NMOS power transistor to 2,000 μm and 0.35 μm, respectively. The sampling frequency of the dynamic biasing network is set to $1/T_S = 100$ kHz and capacitors are set to $C_R = C_S = 5$ pF (the corresponding settling time is $t_s = 40\,\mu$s). In the clock booster, diode D_0 is implemented by a p^+ diffusion in a n-well region, the aspect ratio of M_0 is set to $\frac{60}{0.35}$ and capacitors C_1 and C_2 are set to 0.2 pF and 1 pF, respectively. The two-stage Miller-compensated OTA shown in Fig. 8 is used for the error amplifier. Component values are reported in Table 1.

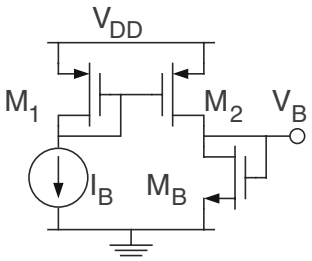

Fig. 7 Circuit for generating voltage V_B

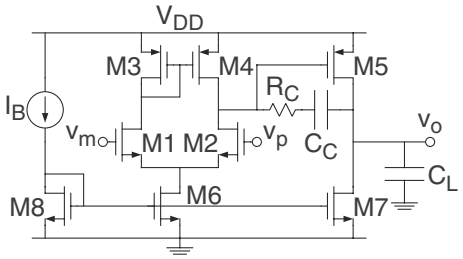

Fig. 8 Schematic of the two-stage operational transconductance amplifier

Table 1 Component values of the two-stage OTA

Component	Value
M1, M2	40/0.35
M3, M4	40/0.6
M5	160/0.6
M6	20/0.6
M7	40/0.6
M8	20/0.6
R_C	2.5 kΩ
C_C	10 pF
I_B	10 μA

The total estimated chip area is about 0.03 mm^2. The quiescent current of the regulator is 70 μA, which is dominated by the currents flowing inside the amplifier (the power for generating the control signals for dynamic biasing is negligible).

4.1 Bandwidth and stability

No external component is required for closed loop stability. The loop gain of the regulator, which was obtained with a 20-pF capacitor and a 10-μA load current at the output node, is shown in Fig. 9. In this condition, the regulator

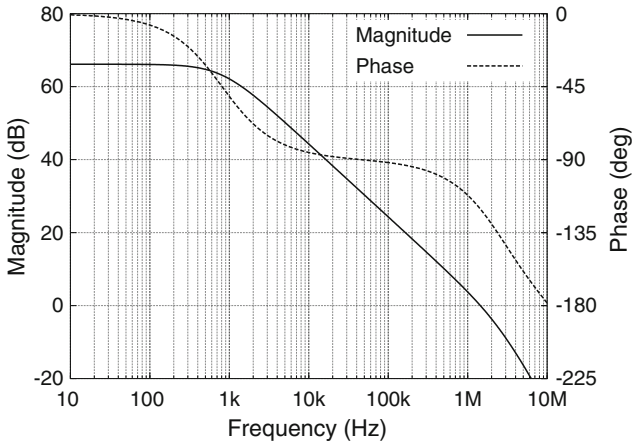

Fig. 9 Worst-case loop gain of the LDO NMOS regulator

exhibits a dc gain of 66 dB and a transition frequency of 1.4 MHz with a 60°-phase margin. The same circuit, loaded with 100 pF, exhibits a phase margin of 31°. Clearly, increasing the load current allows one to increase the load capacitor while maintaining the same phase margin. For example, if the minimum load current is set to 100 μA, the capacitive load may be risen up to 1 nF while maintaining a minimum phase margin of about 30°.

However, since the loop gain is not modified by the introduction of the dynamic biasing technique, the superior stability of NMOS-based regulators (in comparison to PMOS-based ones) is preserved.

4.2 Load and line regulation

Figure 10 shows the output voltage, V_{OUT}, as a function of the load current, I_L, for different values of the supply voltage, V_{DD}. The circuit can deliver 20 mA with a drop-out of 100 mV and 100 mA with a drop-out of 300 mV.

Figure 11 shows the output voltage, V_{OUT}, as a function of the supply voltage, V_{DD}, for different values of the load current, I_L.

4.3 Dynamic biasing

In order to verify the effects of the proposed approach on the speed of the regulator, in this section we report transistor level simulations of the dynamic biasing circuitry including the disoverlapped phases generator and the clock-booster.

The detail of two disoverlapped phases, ϕ_{1n} and ϕ_{2n}, when the circuit is powered at 1.5 V, is shown in Fig. 12. Note that a disoverlap of more than 100 ns is apparent and, as predicted by (13), the clock is boosted up to about $2V_{DD}$.

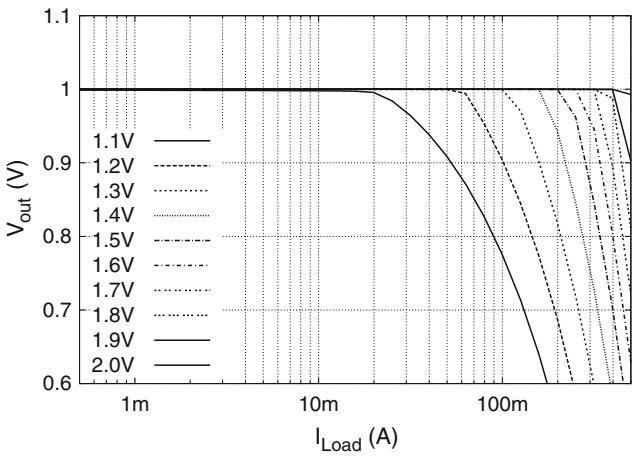

Fig. 10 Output voltage of the proposed NMOS LDO regulator as a function of the load current, for different supply voltages

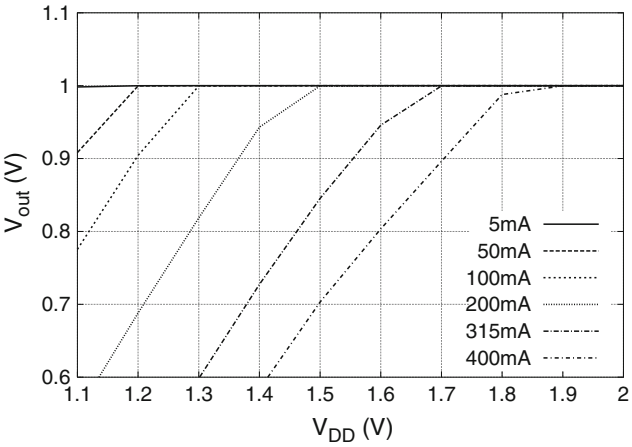

Fig. 11 Output voltage of the proposed NMOS LDO regulator as a function of the supply voltage, for different load currents

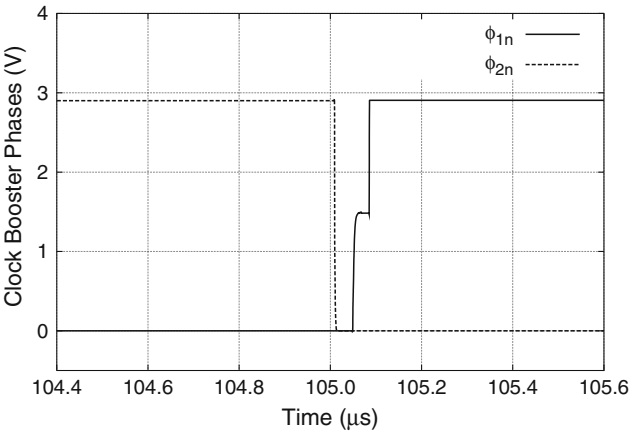

Fig. 12 Detail of the disoverlapped phases

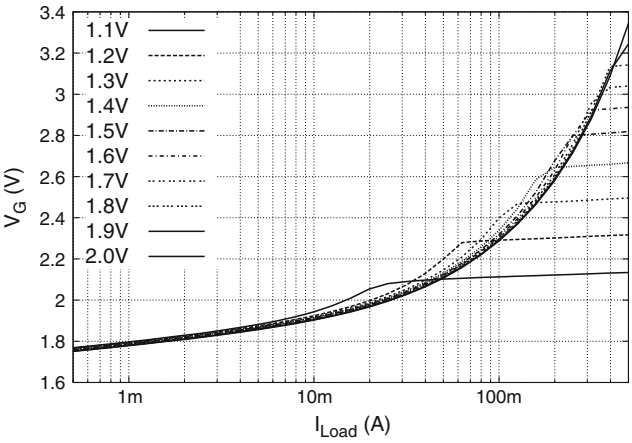

Fig. 13 Voltage applied to the gate of the NMOS power transistor as a function of the load current, for different values of the supply voltage

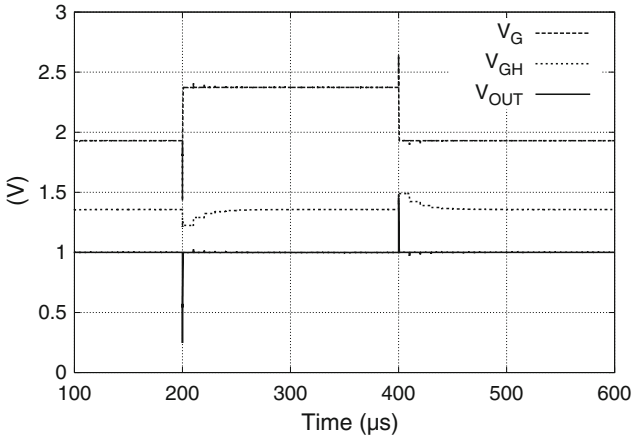

Fig. 14 Transient simulation of a load current change

The static behavior of the gate voltage of M_N (i.e., voltage V_G) as a function of I_L, for different values of the supply voltage, V_{DD} is depicted in Fig. 13. As pointed out before, if V_{DD} drops below 1.4 V (i.e., the desired value for V_B), the shifting capacitor is charged at about V_{DD}. As an example, when $V_{DD} = 1.1$ V, for high load currents the gate voltage may be increased up to about 2.1 V.

In principle, the dynamic biasing strategy does not significantly degrade the speed response of the regulator because, after start-up, the capacitor C_S behaves like a constant voltage source. In fact, Fig. 14 shows $V_{\rm OUT}$, V_G and the voltage across the shifting capacitor, V_{GH}, when the load current is rapidly changed from 10 mA to 100 mA (at time $t = 200\,\mu$s) and vice versa (at time $t = 400\,\mu$s); the reference voltage and the supply voltage are 1 V and 1.5 V, respectively. Inspection of Fig. 14 reveals that, as a consequence of the abrupt current variation, $V_{\rm OUT}$ exhibits negligible voltage spikes of 1 µs duration. Conversely (and as expected), voltage V_G changes rapidly from 1.95 V to 2.35 V (and vice versa) to adequate V_{GS} to the current change. As clearly shown in Fig. 14, the variation of the load current results in sharp variation of the voltage V_{GH} across the shifting capacitor.[2] After the abrupt voltage change, C_S is (slowly) recharged at V_B by the dynamic biasing circuit. This slow process takes about 40 µs, (i.e., the settling time t_s), and is not observable at the output of the regulator because, immediately after the variation, the loop reacts in order to keep the error of the regulator small.

As discussed in Sect. 3.2, Fig. 14 reveals the robustness of the dynamic biasing to switching noise effects, also. In fact, it is apparent that, when the load current changes abruptly (i.e., at time $t = 200\,\mu$s and $t = 400\,\mu$s), capacitor C_S experiences a sharp voltage change. However, the feedback immediately reacts to bring the output voltage to the correct value. The reaction time, which depends on the transition frequency of the feedback loop, is less than 1 μs, in excellent agreement with the simulated transition frequency of 1.4 MHz.

This is evident from Figs. 15 and 16 which show two enlarged views of the same simulation, one for the low-to-high current change and one for the high-to-low change. These figures also show responses of ideal regulators implemented as in Fig. 2 (i.e., with the ideal DC voltage source, V_B). It clearly appears that the effects of the dynamic biasing strategy on the speed of the regulator are irrelevant.

A similar quick reaction occurs for supply voltage variations. It is however interesting to observe that variations of V_{DD} may result in significant variations of V_{GH}; in fact, this is due to the circuit in Fig. 7 which produces $V_B = \min(1.4\text{ V}, V_{DD})$. As an example, Fig. 17 shows $V_{\rm OUT}$, V_G and V_{GH} when the supply voltage is changed from 1.2 V to 1.5 V (at time $t = 200\,\mu$s) and vice versa (at

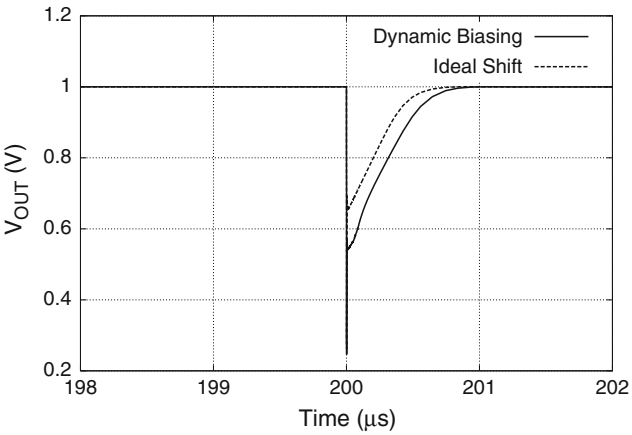

Fig. 15 Detail of transient simulation of a load current change (low-to-high)

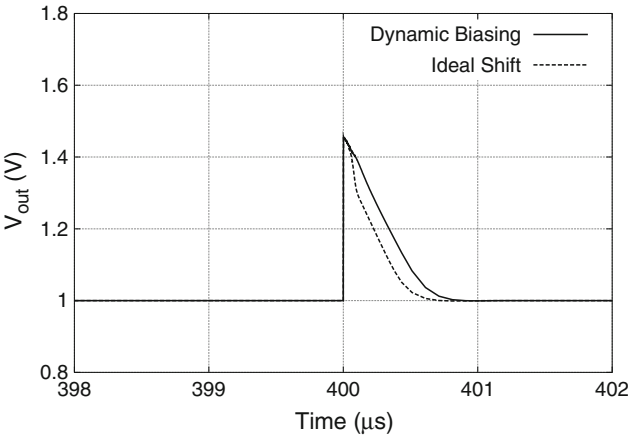

Fig. 16 Detail of transient simulation of a load current change (high-to-low)

[2] Capacitor C_S must supply the charges required for changing V_{GS}, that is, for charging the large capacitor C_{GS} of M_N.

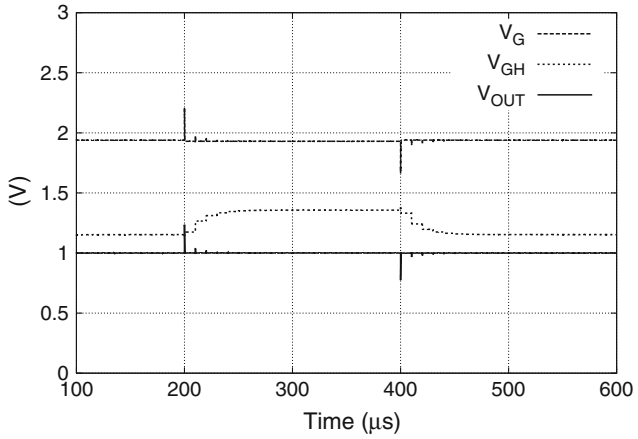

Fig. 17 Transient simulation of a supply voltage change

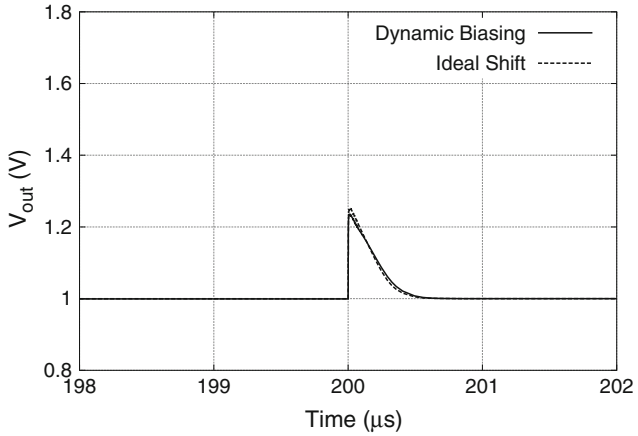

Fig. 18 Detail of transient simulation of a supply voltage change (low-to-high)

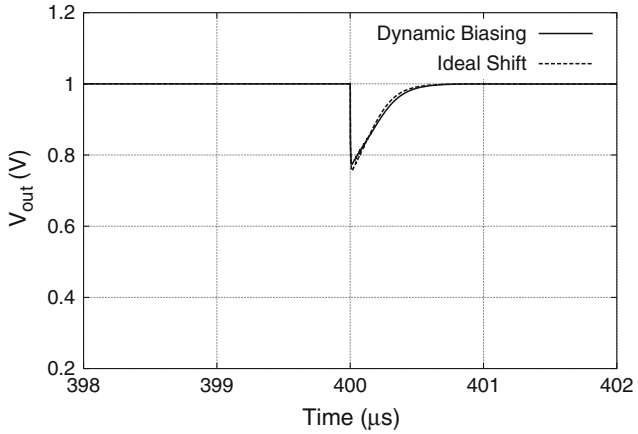

Fig. 19 Detail of transient simulation of a supply voltage change (high-to-low)

time $t = 400\,\mu s$); the reference voltage is 1 V and I_L is maintained at 10 mA. Inspection of Fig. 17 shows that, as expected, both V_{OUT} and V_G remain practically unchanged. Voltage V_{GH}, however, automatically goes (slowly) from V_{DD} to 1.4 V; even in this case the slow charge of C_S is dominated by the settling time t_s but it is not observable at the output node as the loop automatically adjusts the output of the error amplifier in order to keep the error of the regulator small.

This behavior is apparent from Figs. 18 and 19 which show two enlarged views of the same simulation, one for the low-to-high supply voltage change and one for the high-to-low change. The responses of ideal regulators implemented as in Fig. 2 (i.e., with the ideal DC voltage source, V_B) are included, also. It is clearly visible that, again, the effects of the dynamic biasing on the speed of the regulator are negligible.

5 Conclusion

We have proposed a on-chip NMOS low-dropout voltage regulator which exploits a dynamic biasing strategy to properly drive the NMOS output transistor. The circuit does not require external components and is very attractive for on-chip power management. As in two-stages operational amplifiers, the compensation is achieved through an internal Miller capacitor. The dynamic biasing technique, does not affect the speed response of the regulator. Extensive simulations demonstrate the effectiveness and the feasibility of the proposed strategy and the negligible effects of the dynamic biasing strategy on the speed of the regulator.

References

1. Leung, K. N., & Mok, P. K. T. (2003). A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation. *IEEE Journal of Solid-State Circuits, 38*(10), 1691–1702.
2. Hazucha, P., Karnik, T., Bloechel, B. A., Parson, C., Finan, D., & Borkar, S. (2005). Area-efficient linear regulator with ultra-fast load regulation. *IEEE Journal of Solid-State Circuits, 40*(4), 933–940.
3. Tantawy, R., & Brauer, E. J. (2004). Performance evaluation of CMOS low drop-out voltage regulators. In *Proceedings of the IEEE MWSCAS 2004*, Vol. 1, pp. 141–144.
4. Low, A., & Hasler, P. (2004). Basics of floating-gate low-dropout voltage regulators. *Proceedings of the IEEE MWSCAS 2000*, Aug. 2004.
5. Rincon-Mora, G. A., & Allen, P. E. (1998). A low-voltage, low quiescent current, low drop-out regulator. *IEEE Journal of Solid-State Circuits, 33*(1), 1265–1272.
6. Rincon-Mora, G. A., & Allen, P. E. (1998). Optimized frequency shaping circuit topologies for LDOs. *IEEE Journal of Solid-State Circuits, 45*(6), 703–708.
7. Sho, J., Sofer, Y., Polansky, Y., & Maayan, E. (2002). Low power voltage regulator for EPROM applications. In *Proceedings of the IEEE ISCAS 2002*, Vol. 4, pp. 576–579.
8. Gupta, V., Rincón-Mora, G. A., & Raha, P. (2004). Analysis and design of monolithic, high PSR, linear regulators for SoC applications. In *Proceedings of the IEEE International SOC Conference 2004*, pp. 311–315.

9. Heisley, D., & Wank, B. (2000). DMOS delivers dramatic performance gains for LDO regulators. *Electronics Designs, Strategy News, 45*, 141–150.
10. Chava, C. K., & Silva-Martinez, J. (2002). A robust frequency compensation scheme for LDO regulators. In *Proceedings of the IEEE ISCAS 2002*, Vol. 5, pp. 825–828.
11. Lee H., Mok, P. K. T., & Leung, K. N. (2005). Design of low-power analog drivers based on slew-rate enhancement circuits for CMOS low-dropout regulators. *IEEE Transactions on Circuits and Systems II, 52*(9), 563–567
12. Lai, X., Guo, J., Sun, Z., & Xie, J. (2006). A 3-A CMOS low-dropout regulator with adaptive Miller compensation. *Analog Integrated Circuits and Signal Processing, 49*, 5–10.
13. Nebel, G., Baglin, T., San Sebastian, I., Sedlak, H., & Weder, U. (2005). A very low drop voltage regulator using an NMOS output transistor. In *Proceedings of the IEEE ISCAS 2005*, pp. 3857–3860.
14. Bontempo, G., Signorelli, T., & Pulvirenti, F. (2001). Low supply voltage, low quiescent current ULDO linear regulator. In *Proceedings of the IEEE ICECS 2001*, pp. 409–412.
15. Data sheets of REG101, REG102 and REG103 voltage regulators, http://www.ti.com, Texas Instruments.
16. Salmi, K., Scarabello, C., Chevalerias, O., & Rodes, F. (1999). 4V, 5mA low drop-out regulator using series-pass n-channel MOSFET. *Electronics Letters, 35*(15), 1214–1215.
17. Hasler, P., & Low, A. C. (2005). Programmable low dropout voltage regulator. *Proceedings of the IEEE IWSOC 2005*.
18. Giustolisi, G., Palmisano, G., Palumbo, G., & Segreto, T. (2000). 1.2-V CMOS op-amp with a dynamically biased output stage. *IEEE Journal of Solid-State Circuits, 35*(4), 632–636.
19. Unbehauen, R., & Cichocki, A. (1989). *Mos switched-capacitor and continuous-time integrated circuits and systems*. Springer-Verlag.
20. Filoramo, P., Giustolisi, G., Palmisano, G., & Palumbo, G. (2000). Approach to the design of low-voltage SC filters. *IEE Proceedings-Circuits Devices and Systems, 147*(3), 196–200.

Gianluca Giustolisi was born in Catania, Italy, in 1971. He received the Laurea degree (cum laude) in Electronic Engineering from University of Catania in 1995. Up to 1999, he remained, as Ph.D. student, at the Dipartimento Elettrico Elettronico e Sistemistico (DEES) of the same University. In 1999 he received the Ph.D. degree discussing his thesis on the design of a CMOS Fuzzy controller based on the Switched Capacitor approach. In 2002, he joined the Dipartimento di Ingegneria Elettrica Elettronica e dei Sistemi (DIEES) as Assistant Professor. Then he became Associate Professor in 2005. In the academic years 1998/1999 and 1999/2000 he held the course of Microelectronics for the diploma degree in Electronic Engineering. From 2003 to 2005, he held the course of Analog Electronics II for the laurea degree in Automation Engineering. Since 2003 he has been teaching the course of Electronic Devices for the laurea degree in Electronic Engineering. His research interests include analysis, modeling and design of analog integrated circuits and systems with particular emphasis on compensation techniques, Fuzzy integrated circuits, non-linear applications and both low-voltage and low-power circuits. He is author of more than 50 scientific papers on international journals and conferences. He is also author of the textbook Introduzione ai dispositivi elettronici, published by Franco Angeli in 2005.

Christian Falconi was born in Rome, Italy, 1973. He received the M.Sc. (cum laude) and the Ph.D. degrees in Electronic Engineering from the University of Tor Vergata, Rome, Italy, in, respectively, 1998 and 2001; as a part of his Ph.D. program he visited the University of Linkoping (1 month), and TU Delft (7 months). In 2002 he has supervised the design of the electronic interface for the ST-Microelectronics DNA chip. Since 2002 Christian Falconi is Assistant Professor at the Department of Electronic Engineering, University of Tor Vergata, where he teaches Low Voltage Analog Electronics and Fundamental of Electronics. Since 2003 he has been visiting the Georgia Institute of Technology (10 months). His research interests include electronic devices, analog circuits, electronic interfaces, sensors, microsystems, and nanosystems.

Arnaldo D'Amico received the Laurea degree in Physics and Electronic Engineering from the University La Sapienza, Rome, Italy. For several years, he has been with the National Research Council (CNR) leading the Semiconductors Laboratory at the Solid State Electronic Institute, Rome. In 1986, he was appointed Full Professor of electronics at the University of L'Aquila, and, since 1990, he has been with the University of Rome Tor Vergata where he leads the Sensors and Microsystems Group and is Full Professor of electronics, Faculty of Engineering. He teaches courses on electronic devices, microsystems, and sensors. Currently, his main research activities are concerned with the development of physical and chemical sensors, low voltage electronics, noise, and advanced electronic devices. He is author of more than 450 papers in international journals and conference proceedings. He has been Chairman of several conferences on sensors, electronics, and noise and a member of the editorial board of the journals Sensors and Actuators A (physical) and Sensors and Actuators B (chemical). He served as Chairman of the Steering Committee of the Eurosensors conference series from 1999 to 2004. At the national level, he is Chairman of the National Society of Sensors and Microsystems (AISEM) and Director of the Institute of Acoustics "O. M. Corbino" of the National Research Council (CNR).

Gaetano Palumbo was born in Catania, Italy, in 1964. He received the laurea degree in Electrical Engineering in 1988 and a Ph.D. degree from the University of Catania in 1993. Since 1993 he conducts courses on Electronic Devices, Electronics for Digital Systems and basic Electronics. In 1994 he joined the DEES (Dipartimento Elettrico Elettronico e Sistemistico), now DIEES (Dipartimento di Ingegneria Elettrica Elettronica e dei Sistemi), at the University of Catania as a researcher, subsequently becoming Associate Professor in 1998. Since 2000 he is a Full Professor in the same department. His primary research interest has been analog circuits with particular emphasis on feedback circuits, compensation techniques, current-mode approach, low-voltage circuits. Then, his research has also embraced digital circuits with emphasis on bipolar and MOS current-mode digital circuits, adiabatic circuits, and high-performance building blocks focused on achieving optimum speed within the constraint of low power operation. In all these fields he is developing some the research activities in collaboration with STMicroelectronics of Catania. He was the co-author of three books "CMOS Current Amplifiers" and "Feedback Amplifiers: theory and design" and "Model and Design of Bipolar and MOS Current-Mode Logic (CML, ECL and SCL Digital Circuits)" all by Kluwer Academic Publishers, in 1999, 2001 and 2005, respectively, and a textbook on electronic device in 2005. He is the author of 300 scientific papers on referred international journals (over 120) and in conferences. Moreover he is co-author of several patents. Since June 1999 to the end of 2001 and since 2004 to 2005 he served as an Associated Editor of the IEEE Transactions on Circuits and Systems part I for the topic "Analog Circuits and Filters" and "digital circuits and systems", respectively. Since 2006 he is serving as an Associated Editor of the IEEE Transactions on Circuits and Systems part II. In 2005 he was one of the 12 panelists in the scientific-disciplinare area 09-industrial and information engineering of the CIVR (Committee for Evaluation of Italian Research), which has the aim to evaluate the Italian research in the above area for the period 2001–2003. In 2003 he received the Darlington Award. Prof. Palumbo is an IEEE Fellow.