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ScienceDirect
Sensors and Actuators B 129 (2008) 59–66
SENSORS AND ACTUATORS B CHEMICAL
www.elsevier.com/locate/snb

CMOS microsystems temperature control

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Received 1 May 2007; accepted 18 July 2007
Available online 24 July 2007

Abstract

Here we describe a high-accuracy, high-precision interface for the temperature control of a microsystem which contains a bipolar junction transistor for temperature sensing; the desired temperature is set by a digital word and the interface may be integrated in standard CMOS processes. Transistor level simulations of the complete electro-thermal microsystem show that, after a single temperature calibration, the temperature control error may be kept below ±0.1 °C in the temperature range (0 °C–102.4 °C).

Keywords: Temperature control; Electronic interfaces; CMOS microsystems; PTAT sensors; Thermal ΣΔ modulation

1. Introduction

Since physical, chemical, and biological properties generally depend on temperature, temperature control is one of the most important tasks in a huge number of both traditional and emerging applications (pressure sensors, chemical sensors, BioMEMS, DNA chips, μTAS, Lab-on-Chip, etc.). In some cases a rough temperature control is sufficient; in other applications (e.g. pressure sensors) even small errors may reduce the accuracy and precision [1] of the entire system. As a consequence, in many microsystems it is important to control the temperature in a fast, accurate, and precise manner; possibly, the temperature control interface should also be compact, light, cheap, and user-friendly (e.g. programmable). All these requirements may be ideally fulfilled by an integrated CMOS system connected to an external digital system (e.g. a micro-controller), as shown in Fig. 1; if possible, calibration should be unnecessary or, at least, simple. Though a few CMOS interfaces for temperature control [2,3] have been recently reported, there are still a number of open issues.

In general, an automatic temperature regulation system must comprise temperature sensors, thermal actuators, and an electronic interface. Among other options (e.g. temperature dependent resistors), in bipolar, CMOS, or BiCMOS systems, PTAT temperature sensors are almost always preferable because of their better uncalibrated accuracy; furthermore, PTAT sensors may be effectively calibrated with a simple, single temperature calibration procedure. For instance, if resistive temperature sensors are employed [2], the uncalibrated accuracy is obviously poor due to the spread of resistance values and of their temperature dependences; additionally, the calibration procedure could be rather complex; finally, the implementation of temperature-independent current sources may require additional calibration, non-standard processes, or external components (e.g. an external resistor with low temperature coefficient). Though in some cases, resistive temperature sensors might be the only option (e.g. in some cases bipolar junction transistors may not be integrated within the microsystem), if possible, a better uncalibrated accuracy may be achieved by using the base to emitter voltage of a bipolar junction transistor, V_{BE}, for temperature sensing [3]; however, the generation of the "control voltage" to be compared with the voltage V_{BE} would not be straightforward; incidentally, we mention that, for temperature sensing, bipolar junction transistors are generally better than simple pn junctions as collector currents are almost exclusively "diffusion currents" (in contrast with diode currents). As to the actuators, if simplicity and low cost are main issues, "heating actuators" are far more practical than "cooling actuators" because power consuming electronic devices (e.g. resistors or transistors) are natural heaters. As to the electronic interface, it should not degrade the accuracy and precision of the temperature control system; in particular, high-accuracy, high-precision circuit techniques [1] may be necessary; as an example, for CMOS PTAT sensors, the input offset and 1/*f* noise voltages of amplifiers must generally

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doi:10.1016/j.snb.2007.07.071

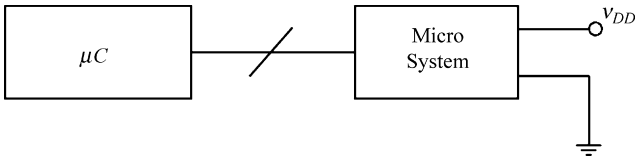

Fig. 1. Smart microsystem temperature control.

be compensated for. The control strategy is also important; in previously reported CMOS interfaces [2,3] for temperature control, the temperature regulation feedback loop is non-linear and, thus, the design may be rather complex; by contrast, although thermal ΣΔ modulation has been originally proposed for smart thermal flow sensors [4,5], we have recently shown that it is also an extremely simple and effective technique for the temperature control of first order (i.e. single pole) thermal systems (for instance, see [6] for the temperature control of the ST DNA chip and [7] for the temperature control of quartz micro-balances).

Here we propose an accurate, precise, fast, and user-friendly CMOS interface for microsystems temperature control; the circuit takes advantage of thermal ΣΔ modulation and comprises a PTAT sensor, an autozeroed comparator, and a digitally tunable, high-precision, high-accuracy bandgap reference. The CMOS chip containing the interface can control its own temperature or the temperature of a second, external microsystem; in the latter case, the external microsystem must contain a bipolar junction transistor acting as the temperature sensor. As a preliminary test, we have designed a temperature control interface in a standard 0.35 μm CMOS process; since our goal here is to demonstrate the feasibility of the general approach rather than a specific application, we neglect area occupation issues and parasitic resistances (e.g. base and emitter resistances might limit the accuracy if the CMOS interface controls the temperature of a remotely located, external microsystem). Assuming a single temperature calibration, transistor level simulations of the complete electro-thermal microsystem show an error below ±0.1 °C in the temperature range (0–102.4 °C).

The paper is organized as follows: Section 2 gives a high-level description of the temperature control system and shows finite elements thermal simulations for a standard packaged CMOS chip; Section 3 describes the CMOS interface for temperature control; Section 4 presents transistor level simulations of the complete electro-thermal system; the conclusions are given in Section 5.

2. High-level system design

Fig. 2 schematically shows the basic principle of a temperature control system which takes advantage of thermal ΣΔ modulation (signals in the thermal domain are modeled by the correspondent signals in an equivalent electric circuit). In practice, the desired chip temperature (set by a digital word) is converted into the voltage v_D which is compared with a PTAT voltage, so that the heaters may be properly enabled or disabled; the ΣΔ loop is intrinsically stable as we assume there is only one dominant pole associated to the (large) thermal time constant $R_{TH}C_{TH}$ (as in many practical cases, e.g. see [6,7]).

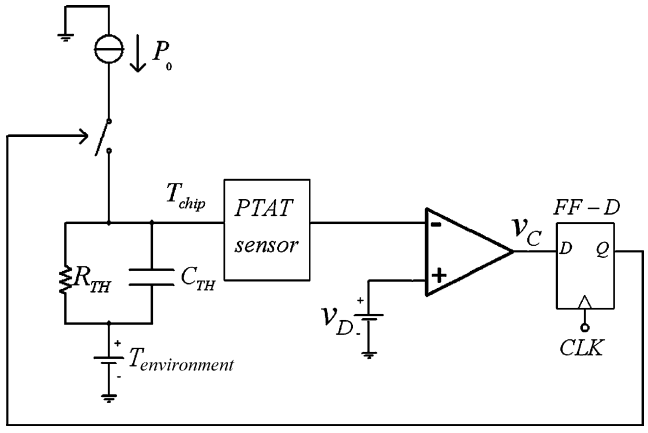

Fig. 2. CMOS temperature control system using thermal ΣΔ modulation (basic principle).

Clearly, the system depicted in Fig. 2 only considers a single temperature for the entire microsystem whose temperature must be controlled; though in many microsystems this assumption would be justified by the high thermal conductivity of silicon, finite elements simulations may provide a more accurate estimation; for instance, Figs. 3–6 show the simulated temperature

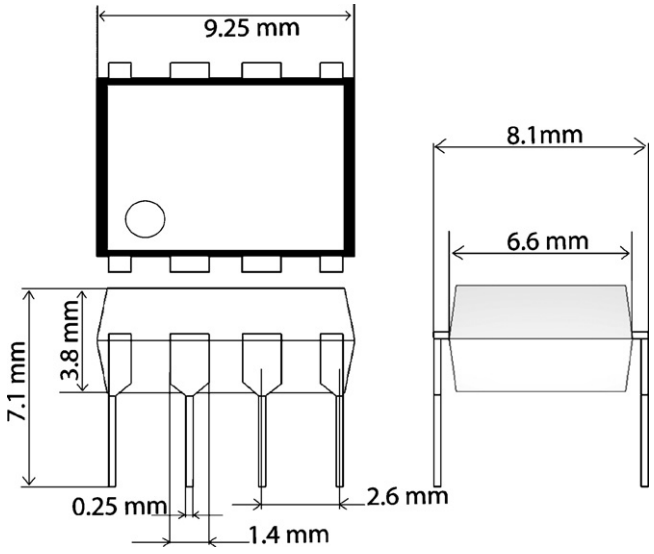

Fig. 3. Dimensions of the standard DIP package which has been used for the thermal finite element simulations of the microsystem.

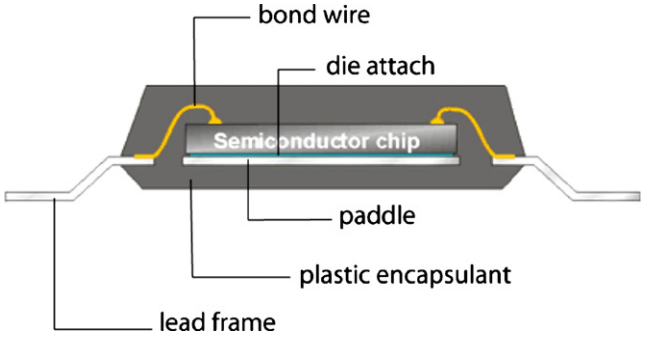

Fig. 4. Section of the packaged microsystem which has been used for the thermal finite element simulations.

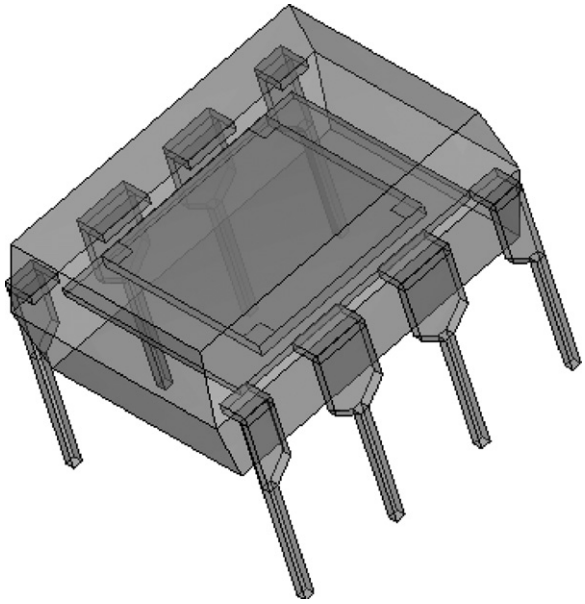

Fig. 5. Three-dimensional view of the packaged microsystem; the squares at the corners of the chip represent the heaters.

distribution (Fig. 6) for a CMOS chip encapsulated into a standard DIP package (Figs. 3–5), heated by a 1 W power, and exposed to an environment temperature equal to 300 K. In the simplified layout the heaters are at the peripheral of the chip and the single temperature sensing transistor Q (see later) is constituted by four shunt connected pnp substrate transistors; in practice the temperature uniformity is very good [8] and the correspondent temperature control error would be negligible for many practical applications.

Accurate PTAT voltages are easily generated in CMOS circuits; in fact, if two currents whose ratio n is accurate are injected into the collectors of two matched bipolar junction transistors, as shown in Fig. 7, the difference between the emitter to base

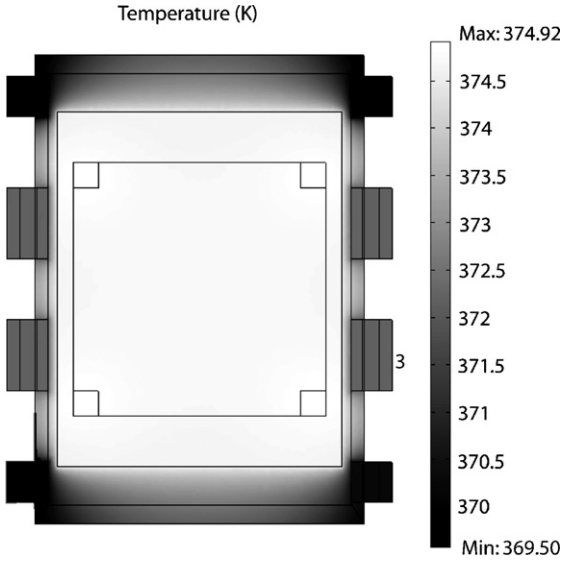

Fig. 6. Temperature distribution in the packaged microsystem.

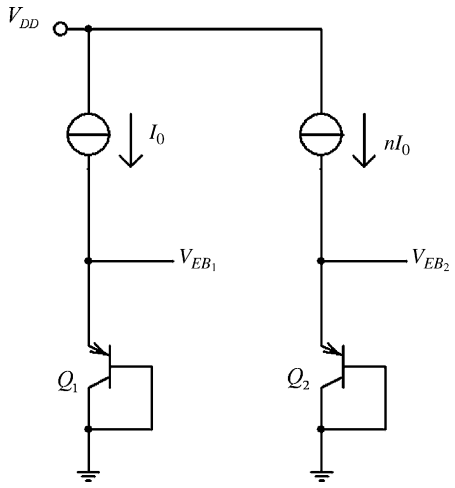

Fig. 7. PTAT technique (basic principle).

voltages of the two transistors is

$$v_{\mathrm{PTAT}} = \frac{k_{\mathrm{B}}T}{q}\ln(n) \tag{1}$$

which is accurately proportional to the absolute temperature, T (k_{B} is the Boltzmann constant, q is the absolute value of the electron charge). In CMOS processes, substrate pnp transistors are very convenient devices for the implementation of PTAT temperature sensors [9–12]. However, mismatch and the existence of even small temperature differences between the two temperature sensing transistors may introduce errors; this is not an issue in most integrated temperature sensors as, first, the two transistors are laid out using a common centroid strategy, second, the power dissipation is rather small (in the μW range), and, third, silicon has a high thermal conductivity. However, in our target application it may be necessary to heat the microsystem well above the external temperature, which may require a high power consumption; therefore, beside a careful layout, it is better to use a single transistor for the generation of the PTAT voltage (see later).

The PTAT voltage must be compared with the voltage v_{D}, whose ideal value is

$$v_{\mathrm{D}} = \frac{k_{\mathrm{B}}T_{\mathrm{D}}}{q}\ln(n) \tag{2}$$

where T_{D} is the desired temperature; as evident from (2), the voltage v_{D} should only depend on the desired temperature T_{D} and *not* on the temperature of the microsystem.

3. CMOS interface for temperature control

In order to validate the proposed approach we have designed the complete control circuitry in a standard 0.35 μm CMOS process, with a supply voltage equal to 2.5 V. In this section we describe the main building blocks, which constitute the interface.

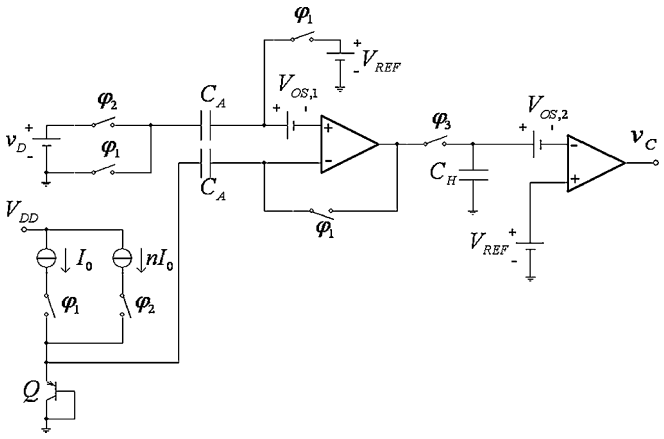

Fig. 8. Comparison between the microsystem temperature and the voltage v_D (autozero comparator).

3.1. Autozero comparator and PTAT voltage step generation

Fig. 8 shows a simplified version of the offset and 1/*f* noise compensated circuit which allows an high-accuracy high-precision comparison between a PTAT voltage step and v_D. The PTAT voltage step is generated by alternatively injecting two different currents into the pnp substrate transistor *Q*, which senses the temperature to be regulated; in this manner a single pnp transistor, *Q*, is used, thus removing errors due to both mismatch and different temperatures of different transistors.

With reference to Fig. 8, the comparator is autozeroed in order to compensate its input offset and 1/*f* noise voltages; each comparator is constituted by a folded cascode op amp, as shown in Fig. 9; during the autozero phase φ_1, the comparator is connected as a buffer (since the pole associated to the output node of the folded cascode op amp is, by far, the dominant pole, there are no stability issues); the circuit topology makes sure that the errors due to the non-idealities of the switches at the input of the comparator are, approximately, common mode errors and, therefore, are rejected. In practice we have used a two-stages autozeroed comparator (i.e. two cascaded comparators identical to the autozeroed comparator shown in Fig. 8)

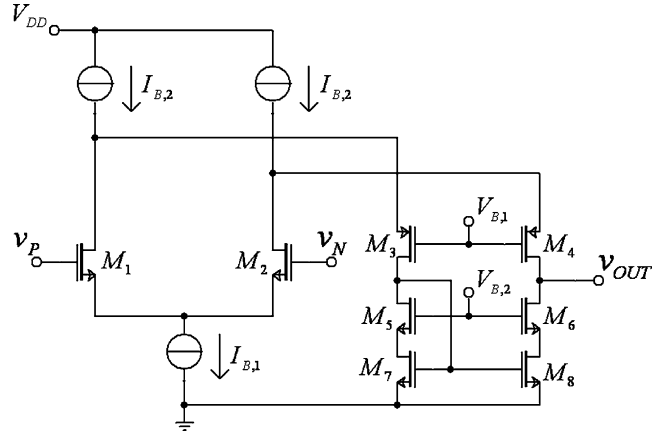

Fig. 9. Folded cascode op amp for implementing the autozero comparator.

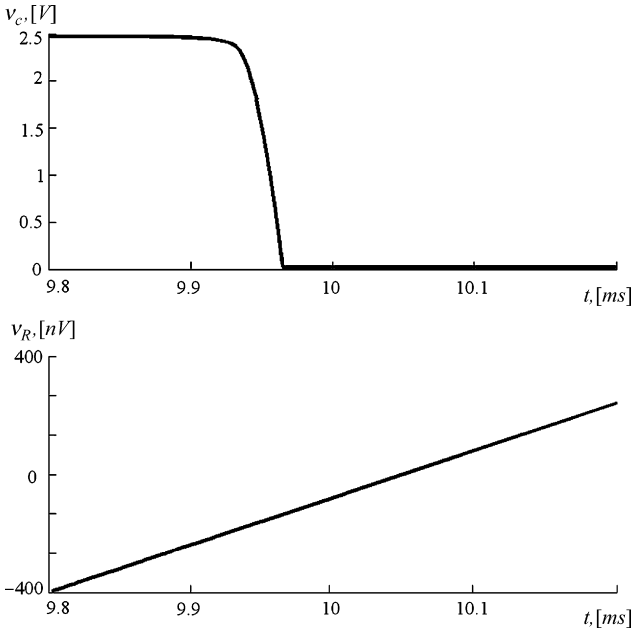

Fig. 10. Autozero comparator simulation.

in order to reduce the residual error originated by the finite gain of the comparator. The capacitor C_H stores the result of the comparison during the autozeroing phases; the voltage v_C controls the heaters (in practice this simple "sample and hold" circuit replaces the D type flip–flop shown in Fig. 2); clearly, the switch φ_3 samples the output of the comparator after transient is exhausted.

The total capacitance value used in the two-stages comparator is equal to 100 pF (we do not focus here on area occupation). Fig. 10 shows the simulated input error voltage of the autozeroed comparator; a dc voltage source equal to 10 mV has been connected in series with the comparator, in order to mimic its input offset; afterwards, a 60 mV step is applied at its non-inverting input and a 60 mV step plus the ramp v_R (see the ramp v_R at the bottom of Fig. 10) is applied at the inverting input, so that the value of v_R when the output of the comparator goes from high to low is the input error voltage of the autozeroed comparator. The simulated input error of the comparator is well below the μV; though this is only an estimation (it is difficult to evaluate channel charge injection and clock feed-through with such accuracy), it is obvious that the input voltage error of the autozeroed comparator will not introduce significant temperature control errors (see later).

3.2. High-accuracy, high-precision, tunable, CMOS bandgap reference

The voltage v_D should only depend on the desired temperature T_D and not on the microsystem temperature, *T*; in practice, v_D must be accurate, precise, and digitally tunable. A simplified circuit for generating the voltage v_D is shown in Fig. 11 (the switches are controlled by the bits B_1). Ideally, the desired temperature (i.e. the temperature when the PTAT voltage and the

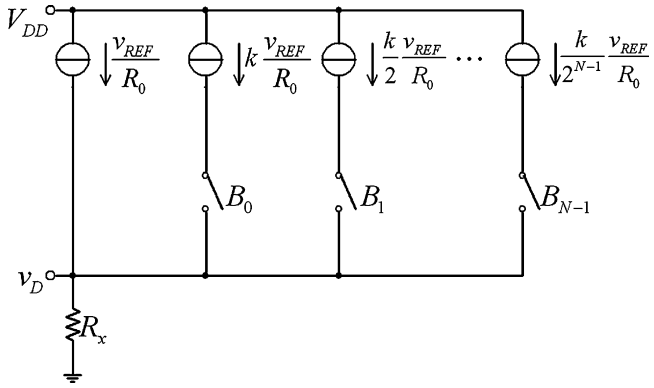

Fig. 11. Circuit for the generation of the voltage v_D.

voltage v_D (2) are exactly equated by the control loop) is

$$T_D = \frac{qV_{REF}}{k_B \ln(n)} \left(\frac{R_X}{R_0}\right) \left(1 + k\sum_{l=0}^{N-1} \frac{B_l}{2^l}\right) \quad (3)$$

where clearly, the ratio between the resistances R_0 and R_X must be as accurate as possible (i.e. these resistors must be of the same type and properly laid out).

PTAT signals are typically rather small; for instance, with $n = 10$ the PTAT voltage is about 60 mV at room temperature and its temperature sensitivity, S_{PTAT}, is about 200 μV/°C. The input voltage error E_C of the comparator and the error E_{VD} of the circuit which generates v_D result in a temperature control error

$$E_T\ (^\circ C) \simeq \frac{E_C + E_{VD}}{S_{PTAT}} \simeq \left(\frac{E_C + E_{VD}}{200\,\mu V}\right) \quad (4)$$

As seen in the previous section, the input voltage error of the autozeroed comparators may be in the μV range and is, therefore, not critical; on the other hand, in order to keep the temperature control error below (x) °C the error of the circuit for generating v_D should be below $(x \times 200)$ μV within all the desired temperature range, which can be difficult; for instance, with x equal to one (i.e. an acceptable temperature control error equal to 1 °C), the error of the circuit for generating v_D should be below 200 μV within all the temperature range. In particular, errors of the bandgap circuit, which generates the current v_{REF}/R_0 are likely to be critical (with proper design and layout, if area occupation is not a main issue, the relative errors of resistor ratios and of current mirrors may be reduced to rather small values).

Fig. 12 shows the bandgap circuit for generating the current v_{REF}/R_0; for simplicity, the start up circuitry is not explicitly shown; the biasing voltage V_B is easily generated by the bandgap circuit itself; attenuated or amplified versions of the current v_{REF}/R_0 are accurately mirrored by cascode current mirrors made by proper connections of well matched unity transistors; the area of the unity transistors must be the minimum area which keeps the mismatch between nominally identical transistors small enough (this area depends on both the process and the current level). The dominant sources of error are likely to be the input offset and 1/f noise voltages of the CMOS op amp;

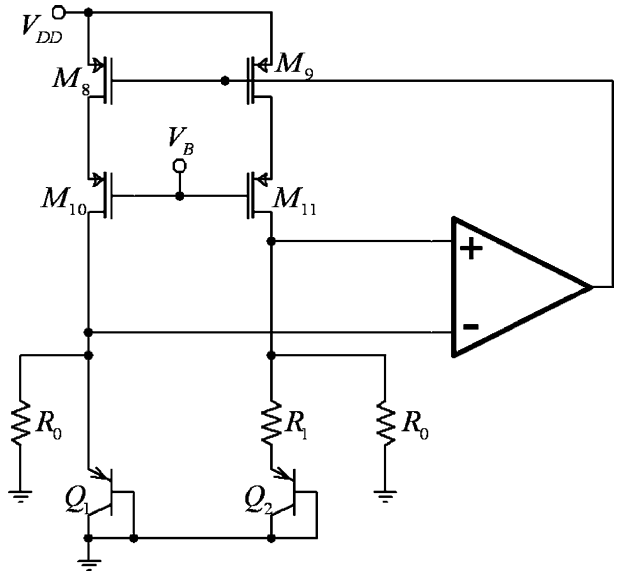

Fig. 12. Bandgap circuit for the generation of v_{REF}/R_0.

both these problems may be compensated by means of chopper or autozero.

The input offset and 1/f noise voltages of CMOS op amps may be compensated by using the amplifier with internal chopper (see [13]) shown in Fig. 13 as the op amp in the v_{REF}/R_0 current source (the chopper switches enable the straight connections in the first phase and the cross-connections in the second phase); clearly, the gain of the chopper op amp shown in Fig. 13 is rather low (the second stage of the op amp has a diode connected transistor as the load); this might seem an important disadvantage, due to the inability of the chopper technique to compensate the finite op amp gain (in contrast with autozero). Nevertheless, if the amplifier shown in Fig. 13 is inserted in the bandgap circuit shown in Fig. 12, the bandgap circuit becomes extremely robust against the finite gain of the op amp. In fact, if we neglect the mismatch between nominally identical transistors, when the input differential voltage of the op amp is zero, the output voltage of the op amp is different from zero (i.e. there is a significant output offset voltage); however, with the correct choice of the

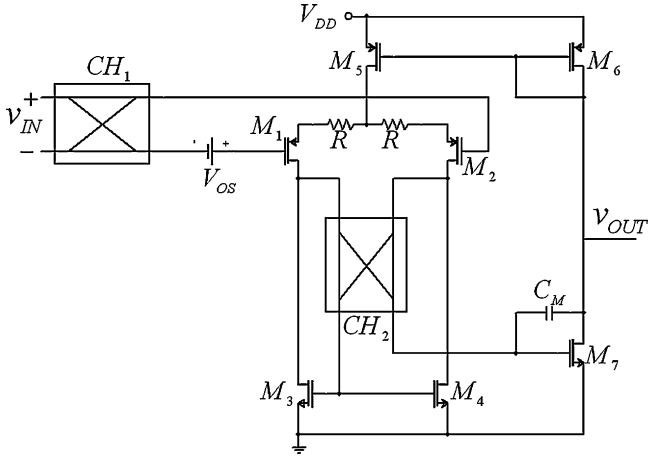

Fig. 13. Amplifier with internal chopper.

transistor widths

$$\frac{W_7}{W_4} = 2\frac{W_6}{W_5} \tag{5}$$

this output offset voltage is exactly the voltage which is required for properly driving the transistors M_8 and M_9 (see Fig. 2); as a result, as long as the mismatch between nominally identical transistors is compensated for, the finite gain of the op amp does not introduce significant errors. Though the input offset and $1/f$ noise voltage of the amplifier are effectively compensated by chopper, there will be a ripple at the output of the op amp and, clearly, this ripple translates into a ripple of the tunable voltage v_D. In fact, (for simplicity, we neglect here the degeneration resistances R, see later) the input stage injects into the Miller capacitor a current $g_m V_{OFF}$ during the first half period and a current $(-g_m V_{OFF})$ during the second half period, where g_m and V_{OS} are, respectively, the transconductance and the input offset voltage of the input stage of the amplifier. Assuming, for the sake of simplicity, a very high gain for the second stage, the gate of M_7 may be considered (dynamically) at virtual ground and, therefore, the peak-to-peak ripple amplitude at the output of the chopper amplifier is approximately

$$V_{OUT,RIPPLE,PP} \simeq \frac{g_m V_{OS}}{2 f_{CH} C_M} \tag{6}$$

where f_{CH} is the chopper frequency. Inspection of (6) shows that the output ripple does not depend on the circuit where the chopper amplifier is inserted and that, though it is possible to reduce the ripple by proper design, there are ultimate limits: a low tail current in the first stage, a small *W/L* ratio, and resistive source degeneration (see Fig. 13) reduce the effective g_m, but there are trade offs with area occupation, noise, and mismatch; the chopper frequency f_{CH} may not be too high in order to limit clock feed-through errors; the Miller capacitance C_M may not be too large (area and rejection of fast disturbances). Though it might be difficult to reduce the ripple of the tunable reference voltage down to negligible levels, in our application the effects of the ripple are not too serious if the comparison between v_D and the PTAT voltage is considered at the most appropriate instant (i.e. in the middle of each ramp); this would, clearly, require a proper synchronization between the ripple and the phase φ_2.

However, an autozero strategy may also be considered; as an example, for our preliminary simulations we have used the autozero bandgap circuit shown in Fig. 14; during the phase φ_1, the sampling capacitor is charged at the V_{OS} voltage; during the phase φ_2, the sampling capacitor is placed in series with the non-inverting input terminal of the op amp, so that the input offset and $1/f$ noise voltages are compensated. Since the gain error is also sampled on the capacitor C_0, this bandgap circuit also compensates the finite gain of the op amp (*gain enhancement*); however, as we have discussed, the finite gain of the op amp does not significantly contribute to the temperature control error. During the phase φ_2 the capacitor C_0 is very slowly discharged (only) by the leakage currents of the (minimum size) switches, so that even relatively low frequency control signals for the switches are acceptable (the leakage currents values should be considered at the highest temperature). The current v_{REF}/R_0

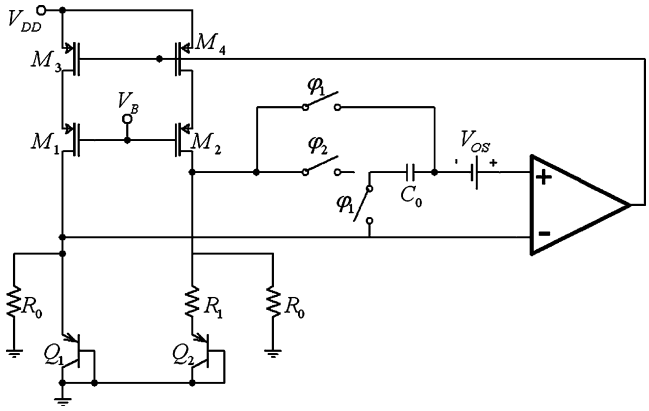

Fig. 14. Autozero bandgap circuit for the generation of v_{REF}/R_0.

is approximately 5.3 μA; the power consumption of the bandgap circuit is not a main issue as a larger power may be necessary for heating the microsystem. In our simulations the autozero frequency is 2 kHz. Fig. 15 shows the ideal reference voltage v_{REF} (i.e. obtained with a grounded nullor instead of the op amp, dotted line), and the voltage v_{REF} produced by the autozero circuit (solid line) when the capacitance C_0 is 40 pF; the input offset voltage of the op amp has been modeled by using $V_{OS} = 5$ mV (see Fig. 14). Although the reference voltage (and, correspondently, the voltage v_D) are accurate only during the phase φ_2, this is not a problem as, with a proper control signal φ_3 the output of the comparator is sampled in the middle of the phase φ_2 (i.e. after the transient originated by the switch commutations is exhausted).

The (simulated) calibration procedure consists in tuning the resistance R_X until the temperature control error at room temperature is zeroed. With this approach, the solid line in Fig. 16 shows the error on v_D at different temperatures; the correspondent temperature control error is below ±0.1 °C in the temperature range (0–102.4 °C) (see (4)) and is largely due to the (undesired) temperature drift of the reference voltage, which may be reduced with a more complex design (the curvature of bandgap references is a systematic error and can, therefore, be compensated for [12,14–16]). We stress that if an accurate and precise volt-

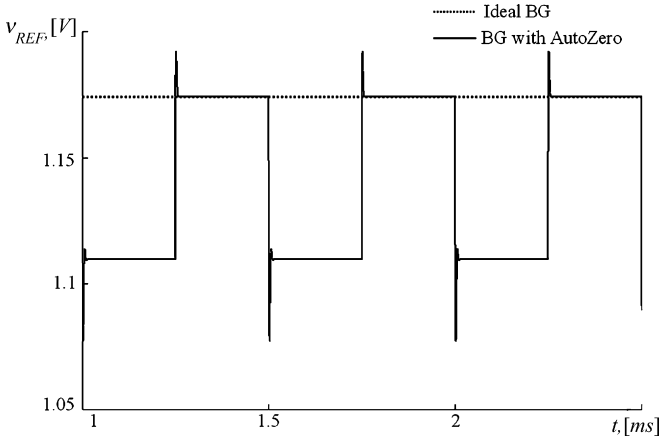

Fig. 15. Ideal reference voltage (dotted line) and reference voltage generated by the autozero bandgap circuit shown in Fig. 14 (solid line).

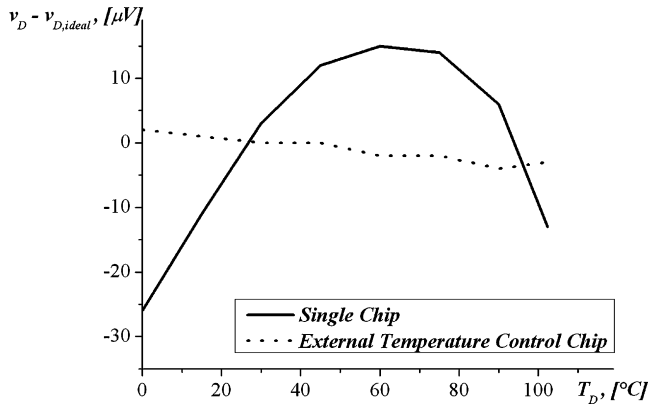

Fig. 16. Error of the circuit for generating the voltage v_D.

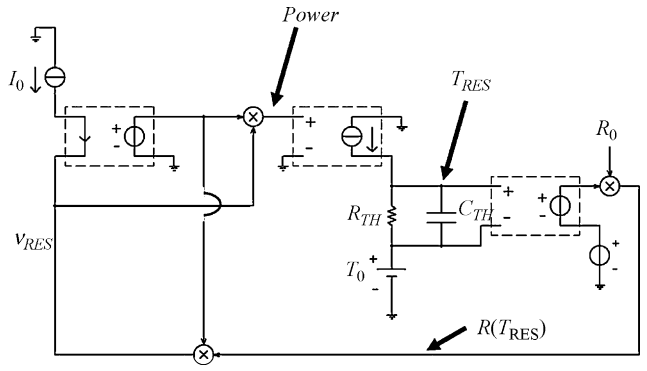

Fig. 17. SPICE model for studying the self-heating of a temperature dependent resistor.

age reference is already available (e.g. the voltage reference is an input to the CMOS chip or an on-chip floating-gate voltage reference), a high-accuracy, high-precision voltage to current converter would be sufficient and there would be no need for calibration. If the CMOS chip temperature is almost constant and the circuit controls the temperature of an external microsystem (instead of its own temperature), the reference voltage would show a much smaller thermal drift and, therefore, the temperature control error would be even smaller; for instance, the dotted line in Fig. 16 shows the error on v_D at different temperatures of the microsystem when the temperature of the CMOS control chip is constant; in this case the estimated temperature control error would be so small that errors of current mirrors and of resistor ratios should be taken into account. Clearly, if the CMOS chip must control the temperature of an external microsystem, the proposed approach would only be acceptable if the external microsystem still contains a bipolar junction transistor; additionally, the errors of parasitic resistances in series with the temperature sensing bipolar junction transistor should be considered.

4. Complete system simulation

As in many electronic interfaces design [1], the simulation of the complete system requires a model for signals and systems outside the electrical domain. Almost always, the most practical solution is to model non-electrical signals and systems by means of equivalent signals and systems in the electrical energy domain, so that the complete system may be analyzed by means of standard simulators for electronic circuits such as SPICE; in fact, though one could conceive a dual approach (modelling electrical signals and systems by means of equivalent signals and systems in different energy domains), the "superior" performance of electronic circuits simulators and the complexity of analog circuits and electronic devices make such an approach useless. A given thermal system may be translated into an equivalent electric circuit by using the following equivalence table:

$$P \leftrightarrow I, \qquad \Delta T \leftrightarrow \Delta V, \qquad R_{TH} \leftrightarrow R, \qquad C_{TH} \leftrightarrow C \quad (7)$$

where for each signal or component in the thermal domain (left) there is an associated electrical signal or component in the electrical domain (right). For our target application, the thermal conductivity of silicon is so high that in many practical cases we may consider a uniform temperature along the entire microsystem, as demonstrated in Section 2; we however mention that this is not general, as, for instance, in some microsystems etching the substrate (bulk micromachining) may increase the thermal resistance between different parts of the microsystem by orders of magnitude. However, for our preliminary tests, we considered the simple model shown in Fig. 2. An additional problem is the need for simulating a time-varying temperature; this is solved by taking advantage of "analog behavioural models" for building SPICE models of bipolar junction transistors with a time-dependent voltage acting as the temperature; this approach is illustrated in Fig. 17 which, as an example, shows a SPICE model for studying the self-heating of a resistor having the resistance which depends on the temperature T_{RES} in a linear manner: the voltage across the resistor, v_{RES}, is computed as the product of the current through the resistor, I_0, and the temperature dependent resistance; it must be stressed that in these equivalent electric circuits there may be no coherence for the dimensions of the various signals; for instance, the signal labelled with *"Power"* is, within the circuit simulator, a *voltage*. By using a similar model for the temperature sensing bipolar junction transistor, the complete electro-thermal system has been simulated. Fig. 18 shows the chip temperature during and after transient (the ideal temperature is 40 °C) when

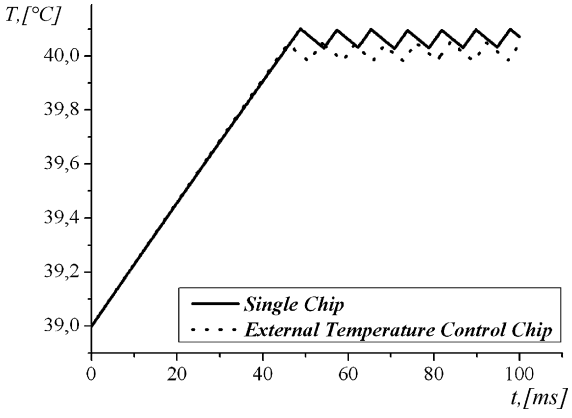

Fig. 18. Simulation of the complete electro-thermal microsystem (desired temperature equal to 40 °C).

the CMOS chip controls its own temperature (solid line) and the temperature of an external microsystem during and after transient.

5. Conclusions

In this paper we have described a CMOS interface which takes advantage of both high-accuracy, high-precision circuit design techniques and of thermal $\Sigma\Delta$ modulation for controlling its own temperature or the temperature of an external microsystem containing a temperature sensing bipolar junction transistor. As long as the microsystem whose temperature must be controlled may be considered a first order thermal system, there are no stability issues. Furthermore, we have identified the main sources of errors (tunable voltage generation, PTAT voltage generation, comparator) and, correspondently, appropriate solutions have been adopted for improving the accuracy and precision of the temperature control: first, we have introduced a digitally tunable, high-accuracy, high-precision bandgap voltage reference; second, a single pnp substrate transistor is used for generating the PTAT voltage step, thus removing errors due to unavoidable mismatch and small temperature differences between different transistors; finally, the comparator is autozeroed. In order to test the complete system, we have designed the control circuit in a standard 0.35 μm CMOS process; neglecting the mismatch-errors of current mirrors and resistor ratios (which corresponds to "waste" enough silicon area for integrating these devices) and assuming a single temperature calibration, transistor level simulations of the complete electro-thermal microsystem show that a temperature control error as low as $\pm 0.1\,^{\circ}$C may be achieved in the temperature range (0–102.4 °C), demonstrating the validity of the proposed approach for a variety of applications (e.g. pressure sensors, chemical sensors, DNA chips, Lab-on-Chip, BioMEMS, μTAS, etc.).

Acknowledgments

Andrea Mauri performed the finite element simulations of the packaged microsystem temperature; Daniele Mazzieri contributed to the design of the autozeroed comparator. The authors also acknowledge Prof. Arnaldo D'Amico, Vincenzo Stornelli, Andrea De Marcellis and Prof. Giuseppe Ferri for stimulating discussions.

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Biographies

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